ASB05V5LCDF

Bi-directional TVS Diode for ESD Protection

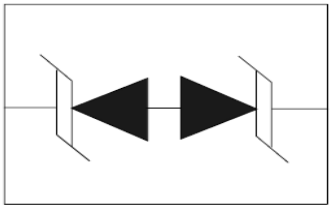
Features

- Ultra-low capacitance: C_J = 10pF typ
- Stand-off voltage: ±5.5V Max
- Solid-state silicon technology
- Low leakage current
- Low clamping voltage: V_{CL} =11.0V typ. @ I_{PP} = 16A (TLP)
- Compliant to Halogen-free

DFN-2L(0402)

Protection Solution to Meet

- IEC 61000-4-2 (ESD)±30kV (Contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Surge) 6A (8/20μs)



Pin Configuration

Mechanical Data

- **Package:** DFN-2L
- **Terminals**: Tin plated lead, solderable per J-STD-002 and JESD22-B102
- **Marking code：** 6A

Maximum Ratings

PARAMETER	SYMBOL	Rating	UNIT
Peak pulse power (t_p = 8/20μs)	P_{pk}	72	W
Peak pulse current (t_p = 8/20μs)	I_{PP}	6	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±30	KV
ESD according to IEC61000-4-2 contact discharge		±30	KV
Junction temperature	T_J	125	°C
Operating temperature	T_{OP}	-40~85	°C
Storage temperature	T_{STG}	-55~150	°C

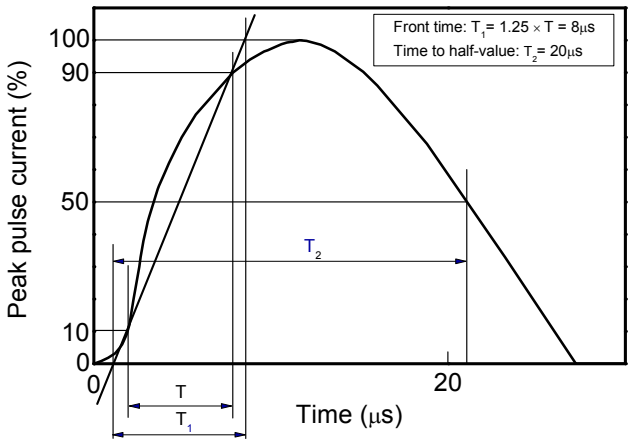
Electrical Characteristics（T_a=25℃ Unless otherwise specified）

PARAMETER	Symbol	UNIT	Conditions	Min	Typ	Max
Reverse maximum working voltage	V_{RWM}	V				±5.5
Reverse leakage current	I_R	nA	V_{RWM} =5.5V			100
Reverse breakdown voltage	V_{BR}	V	I_{BR} = 1mA	6.1	7	
Reverse holding voltage	V_{HOLD}	V	I_{HOLD} = 50mA	6.1	7	
Clamping voltage [1)]	V_{CL}	V	I_{PP} = 16A, t_p = 100ns		11.0	
Dynamic resistance [1)]	R_{DYN}	Ω			0.28	
Clamping voltage [2)]	V_{CL}	V	V_{ESD} = 8kV		11.0	
Clamping voltage [3)]	V_{CL}	V	I_{PP} = 1A, t_p = 8/20μs			8
		V	I_{PP} = 6A, t_p = 8/20μs			12
Junction capacitance	C_J	pF	V_R = 0V, f = 1MHz		10	13
		pF	V_R = 2.5V, f = 1MHz		8	11

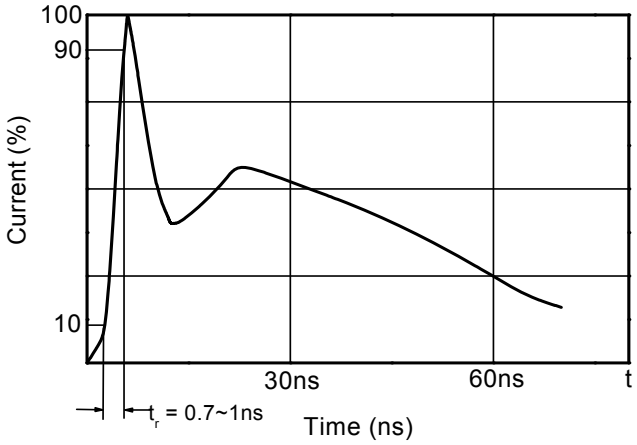
(1). TLP parameter: Z_0 = 50Ω, t_p = 100ns, t_r = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.
(2). Contact discharge mode, according to IEC61000-4-2.
(3). Non-repetitive current pulse, according to IEC61000-4-5.

Typical Characteristics

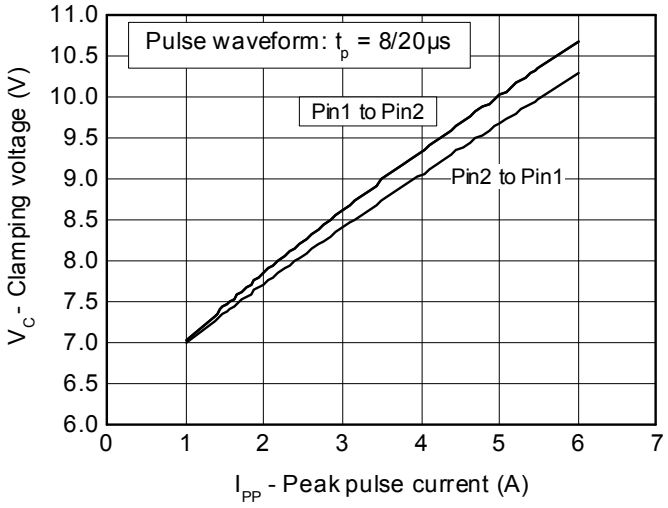
8/20μs waveform per IEC61000-4-5



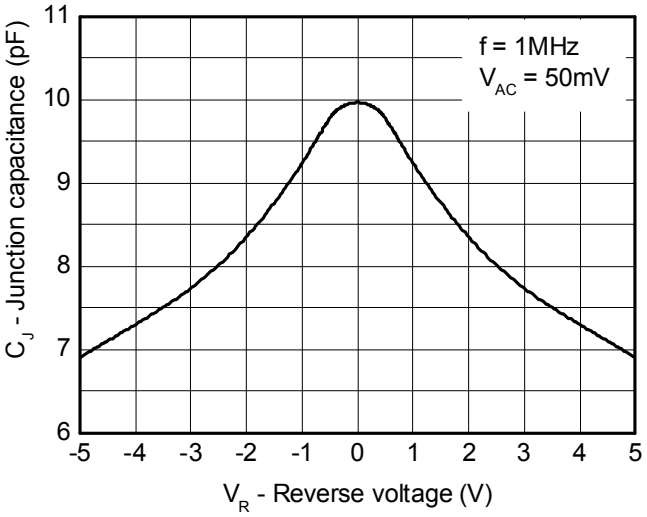
Contact discharge current waveform per IEC61000-4-2



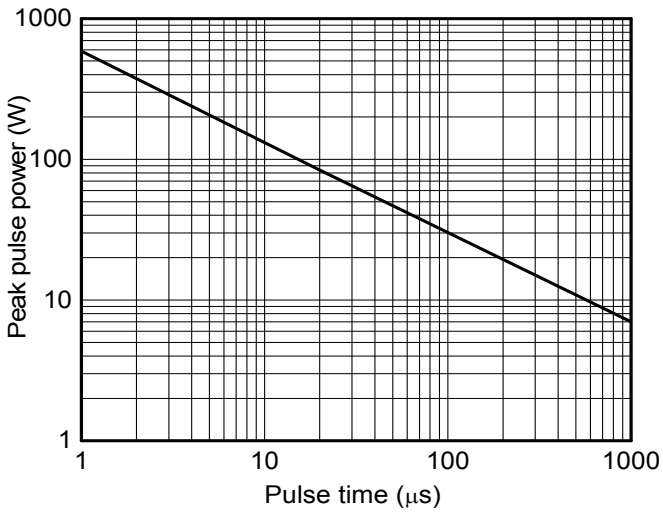
Clamping voltage vs. Peak pulse current



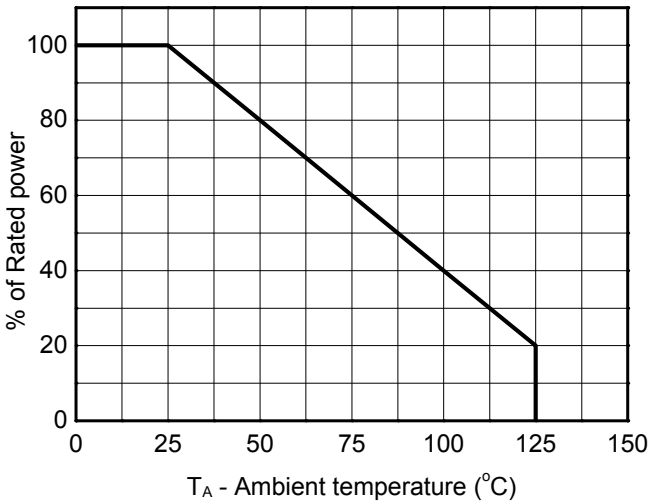
Capacitance vs. Reverse voltage



Non-repetitive peak pulse power vs. Pulse time

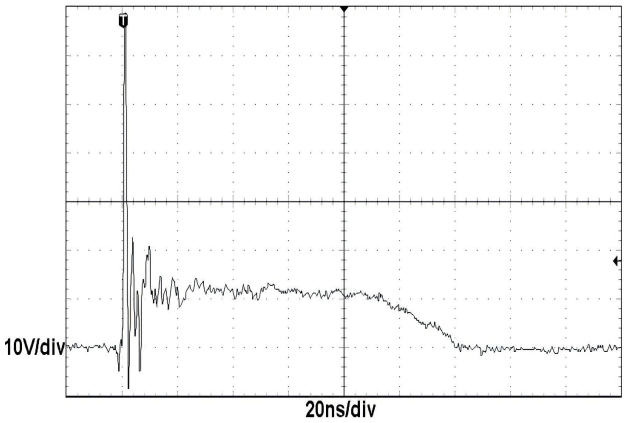


Power derating vs. Ambient temperature



Typical Characteristics

ESD clamping
(+8kV contact discharge per IEC61000-4-2)



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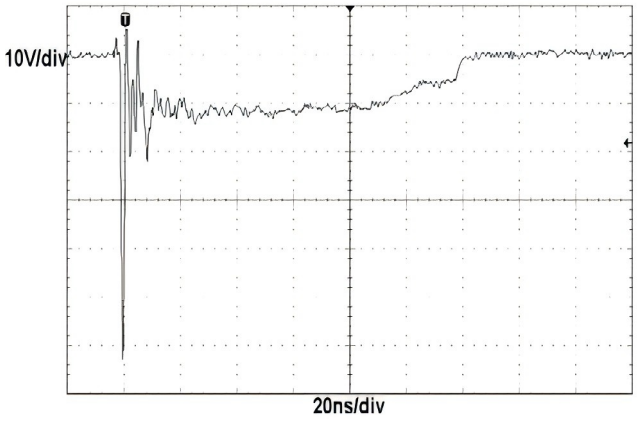
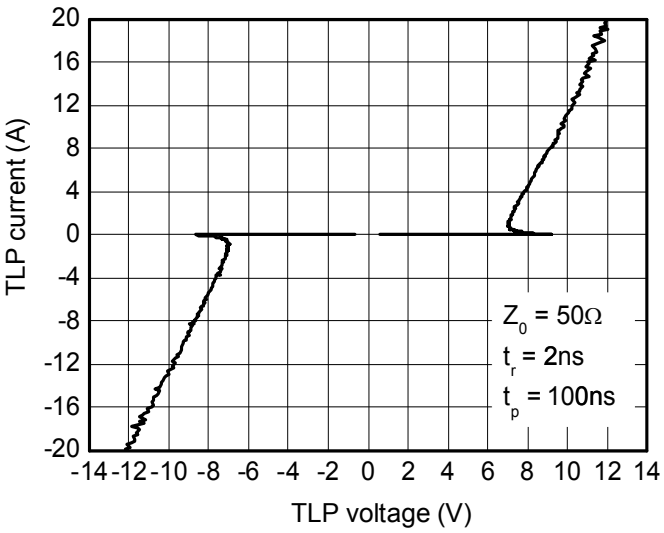
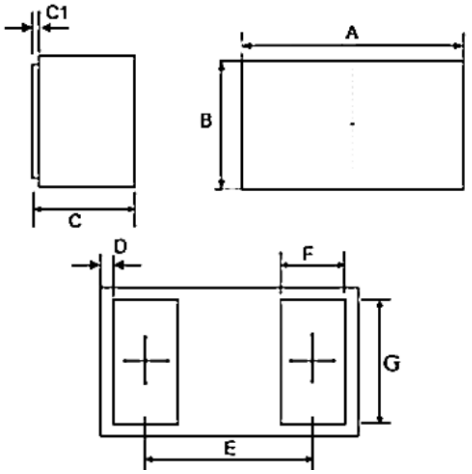


TLP Measurement

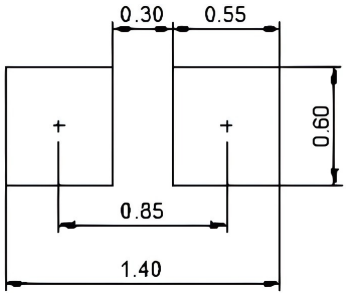


DFN-2L Package Dimensions



Symbol	min. (mm)	Max. (mm)
A	0.95	1.05
B	0.55	0.65
C	0.4	0.5
C1		0.05
D	0.01	0.08
E		0.65
F	0.2	0.3
G	0.45	0.55

Recommend land pattern (Unit:mm)



Notes:
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.