

### Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	$I_D$	$V_{(BR)DSS}$	$R_{DS(on)MAX}$	$I_D$
60V	28mΩ@10V	5A	-60V	80mΩ@-10V	-4A
	38mΩ@4.5V				

### Feature

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and cur
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Suffix "-Q1" for AEC-Q101

### Application

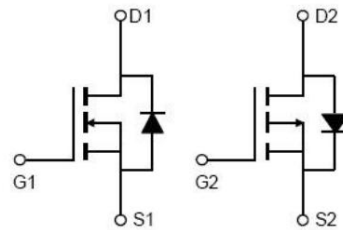
- H-bridge
- Inverters

### Package



SOP-8

### Circuit diagram



### Marking



### Absolute maximum ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N-Channel	p-Channel	Unit
Drain-Source Voltage	$V_{DS}$	60	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current	$I_D$	5	-4	A
Pulsed Drain Current <sup>1)</sup>	$I_{DM}$	30	-30	A
Power Dissipation	$P_D$	2	2	W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	$^\circ\text{C/W}$
Junction Temperature	$T_J$	150	150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55 ~ +150	-55 ~ +150	$^\circ\text{C}$

### N-CH Electrical characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	60			V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$			1	$\mu\text{A}$
Gate-body leakage current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
Gate threshold voltage <sup>2)</sup>	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	1.6	2.5	V
Drain-source on-resistance <sup>2)</sup>	$R_{DS(on)}$	$V_{GS}=10V, I_D=5A$		24	28	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=5A$		32	38	$\text{m}\Omega$
<b>Dynamic characteristics<sup>3)</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V, f=1\text{MHz}$		979		pF
Output Capacitance	$C_{oss}$			120		
Reverse Transfer Capacitance	$C_{rss}$			100		
Total Gate Charge	$Q_g$	$V_{DS}=30V, V_{GS}=10V, I_D=5A$		22		nC
Gate-Source Charge	$Q_{gs}$			3.3		
Gate-Drain Charge	$Q_{gd}$			5.2		
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V$ $R_L=2.5\Omega, R_{GEN}=3\Omega$		4.2		nS
Turn-on rise time	$t_r$			3.4		
Turn-off delay time	$t_{d(off)}$			16		
Turn-off fall time	$t_f$			2		
<b>Source-Drain Diode characteristics</b>						
Diode Forward Current	$I_S$				5	A
Diode Forward voltage <sup>2)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=5A$			1.2	V

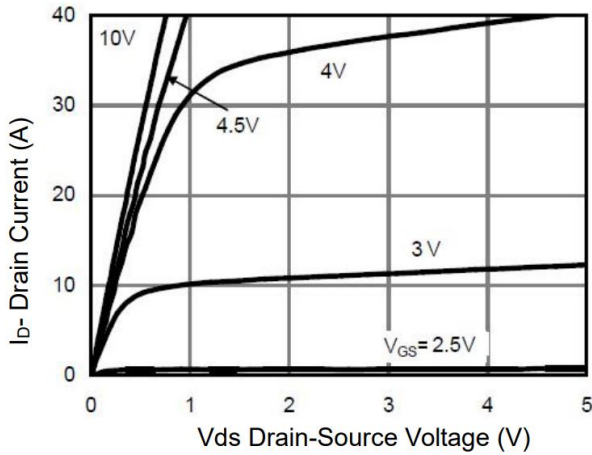
### P-CH Electrical characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-60			V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -60V, V <sub>GS</sub> = 0V			-1	μA
Gate-body leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
Gate threshold voltage <sup>2)</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1.5	-2.6	-3.0	V
Drain-source on-resistance <sup>2)</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -4A		64	80	mΩ
<b>Dynamic characteristics<sup>3)</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V, f = 1MHz		960		pF
Output Capacitance	C <sub>oss</sub>			86		
Reverse Transfer Capacitance	C <sub>rss</sub>			38		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -4A		15.8		nC
Gate-Source Charge	Q <sub>gs</sub>			3		
Gate-Drain Charge	Q <sub>gd</sub>			3.5		
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30V, V <sub>GS</sub> = -10V, R <sub>L</sub> = 2.5Ω, R <sub>GEN</sub> = 3Ω		9		nS
Turn-on rise time	t <sub>r</sub>			10		
Turn-off delay time	t <sub>d(off)</sub>			25		
Turn-off fall time	t <sub>f</sub>			11		
<b>Source-Drain Diode characteristics</b>						
Diode Forward Current	I <sub>S</sub>				-4	A
Diode Forward voltage <sup>2)</sup>	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -4A			-1.2	V

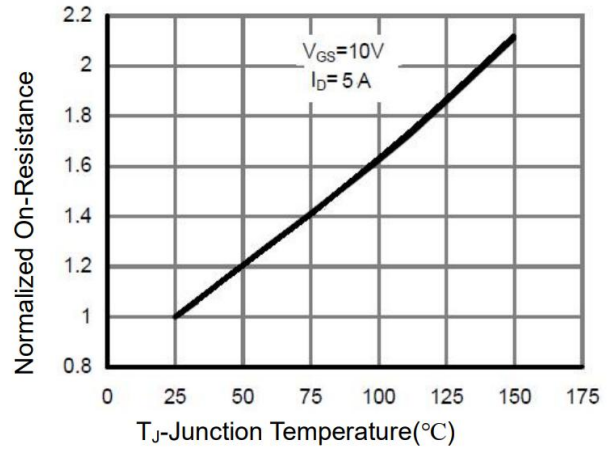
Notes:

- 1) Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2) Pulse Test: Pulse Width < 300μs, Duty Cycle ≤2%.
- 3) Guaranteed by design, not subject to production.

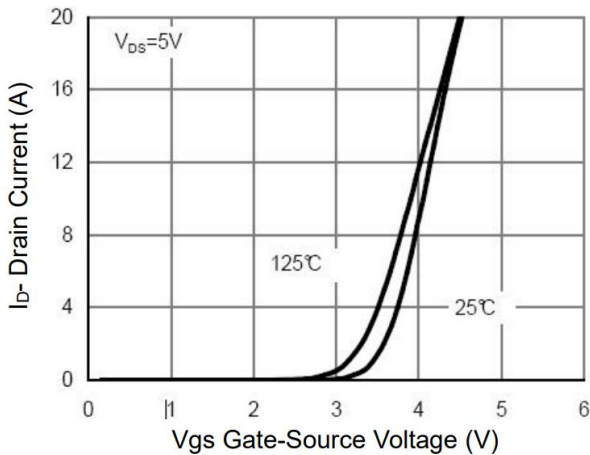
## N- Channel Typical Characteristics



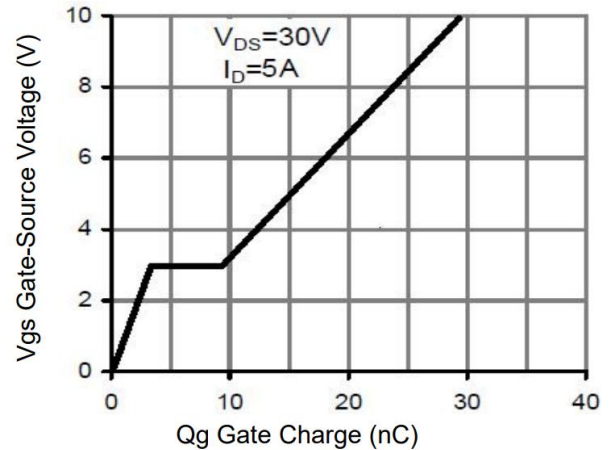
**Figure 1 Output Characteristics**



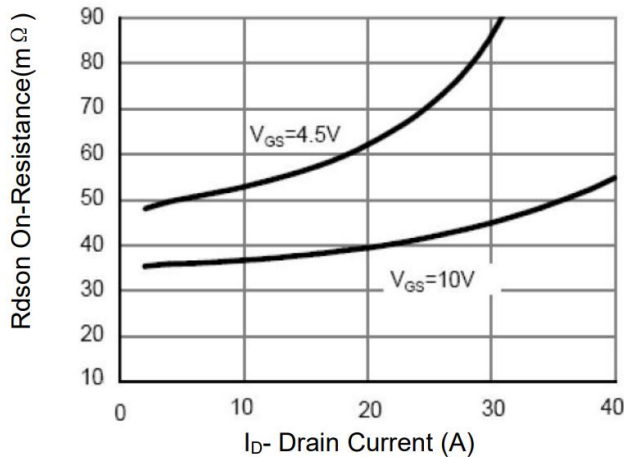
**Figure 2 Rdson-Junction Temperature**



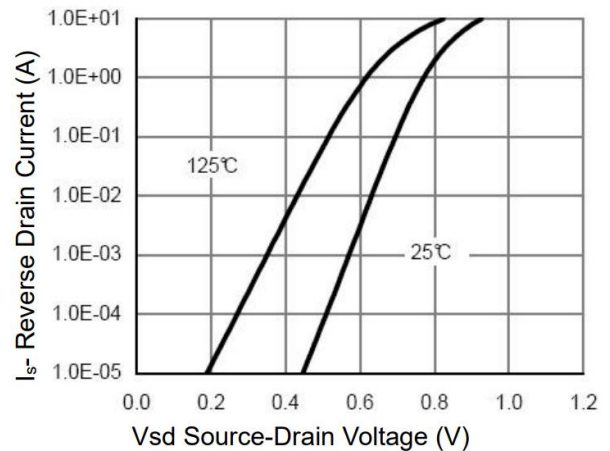
**Figure 3 Transfer Characteristics**



**Figure 4 Gate Charge**

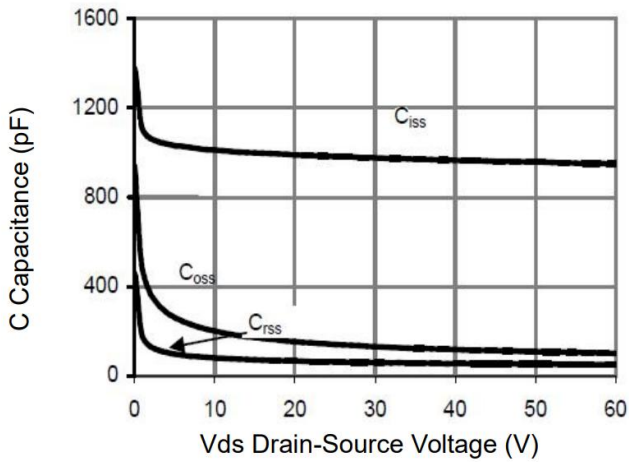


**Figure 5 Rdson- Drain Current**

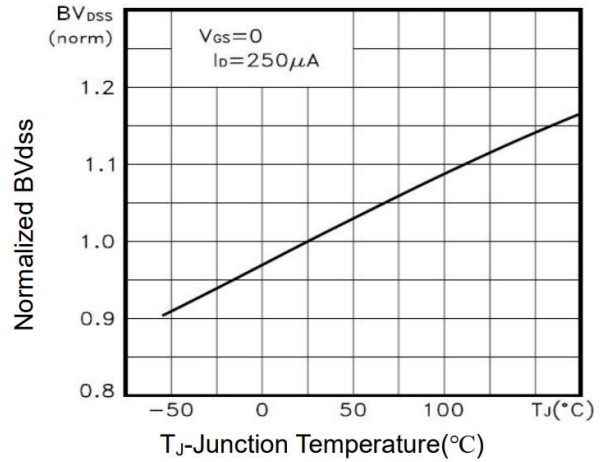


**Figure 6 Source- Drain Diode Forward**

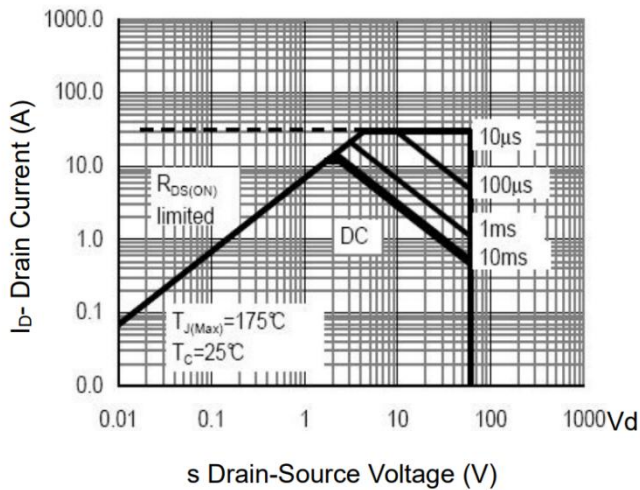
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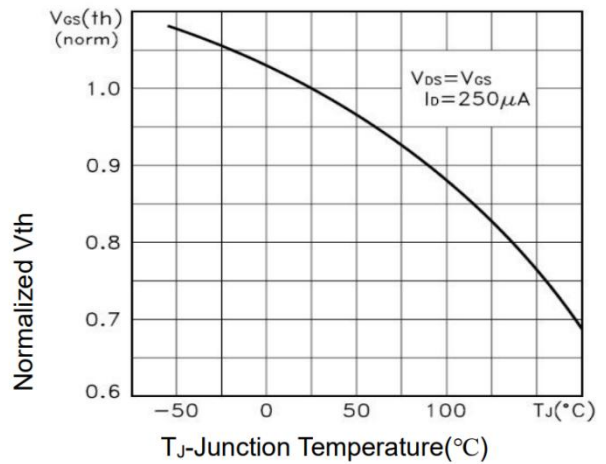
**Figure 7 Capacitance vs Vds**



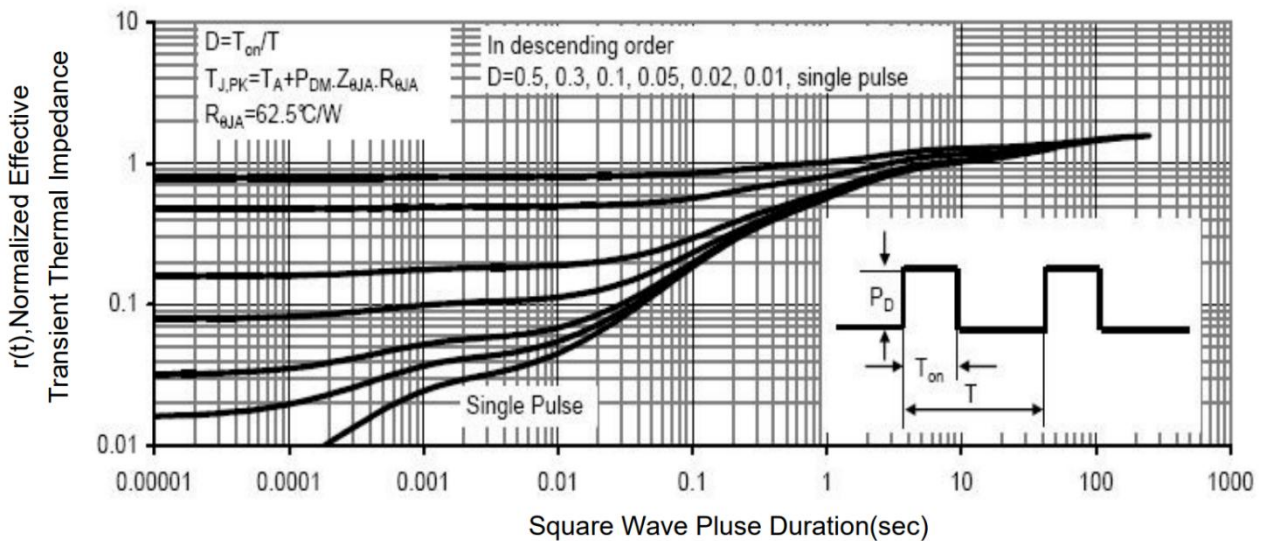
**Figure 8 BV<sub>DSS</sub> vs Junction Temperature**



**Figure 9 Safe Operation Area**

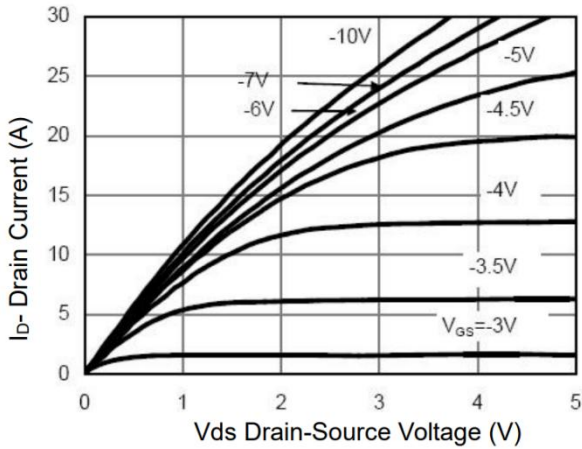


**Figure 10 V<sub>GS(th)</sub> vs Junction Temperature**

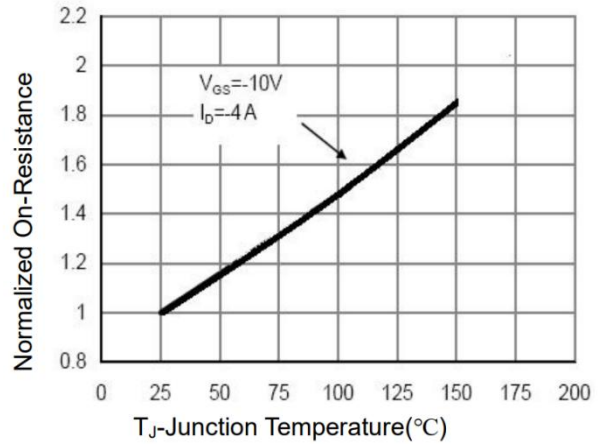


**Figure 11 Normalized Maximum Transient Thermal Impedance**

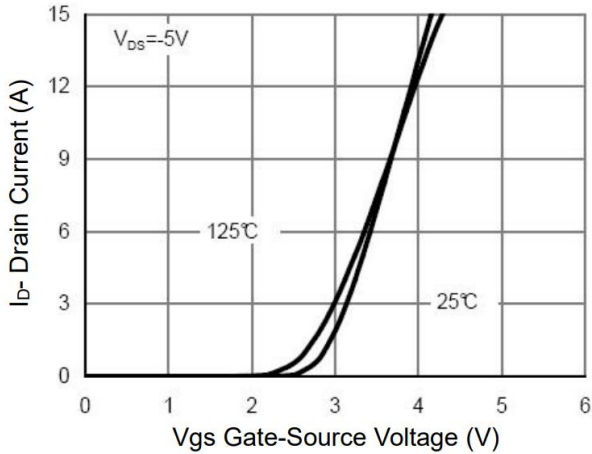
## P- Channel Typical Characteristics



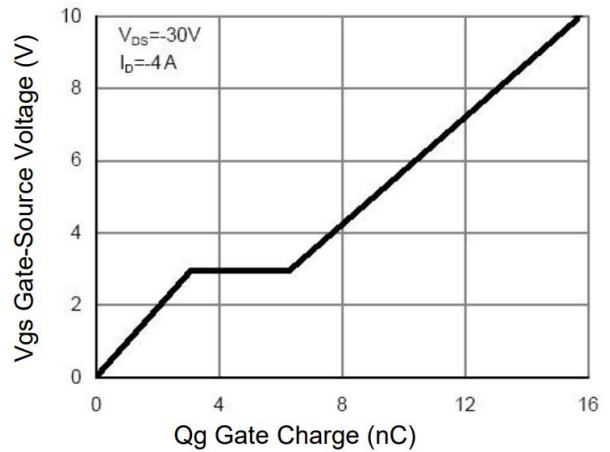
**Figure 1 Output Characteristics**



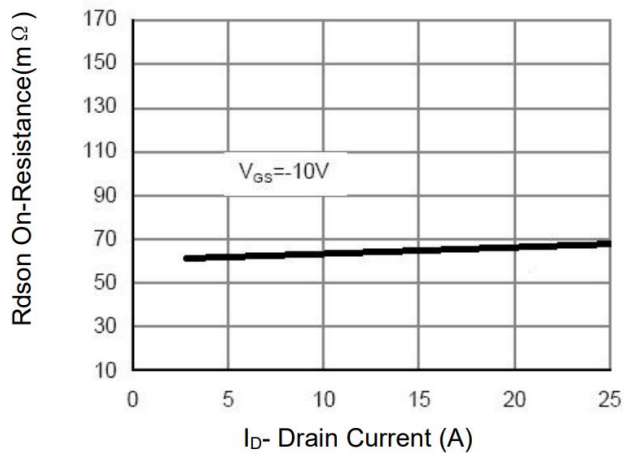
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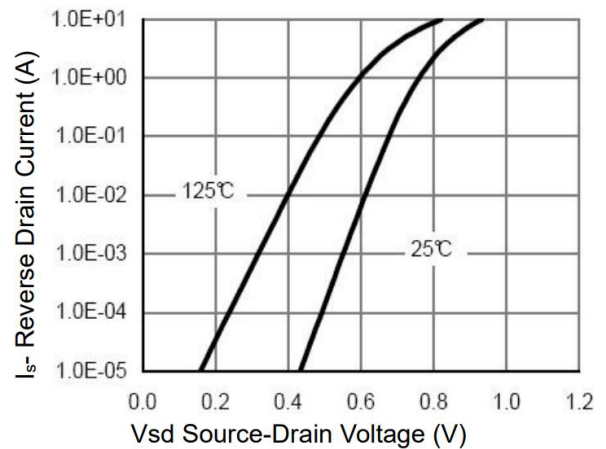
**Figure 3 Transfer Characteristics**



**Figure 4 Gate Charge**

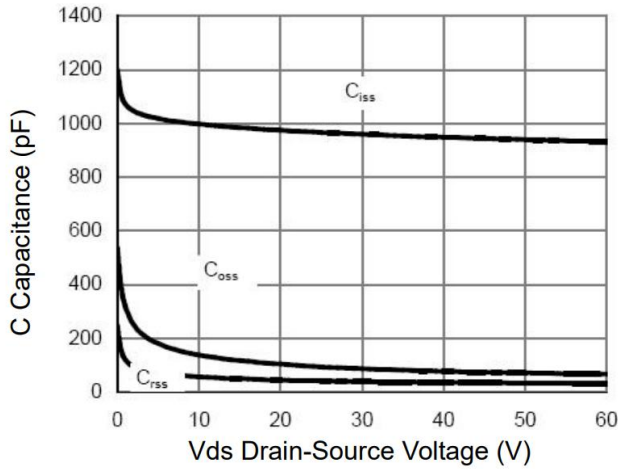


**Figure 5 Rdson- Drain Current**

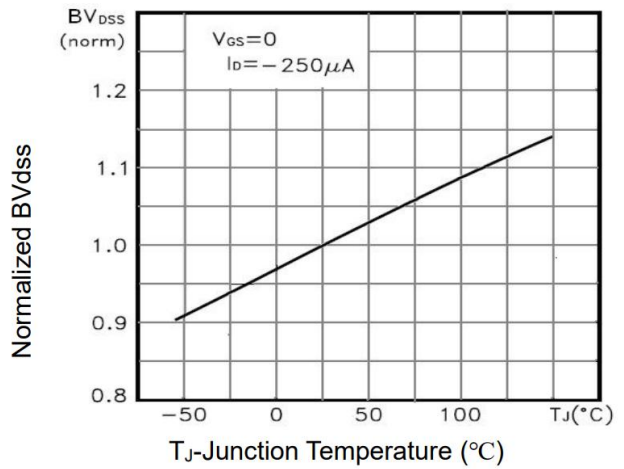


**Figure 6 Source- Drain Diode Forward**

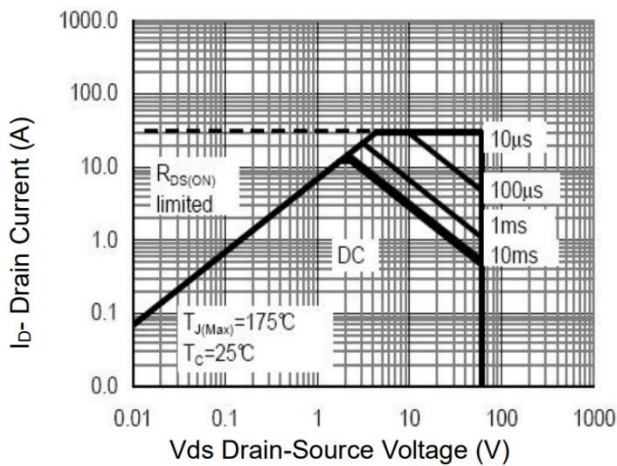
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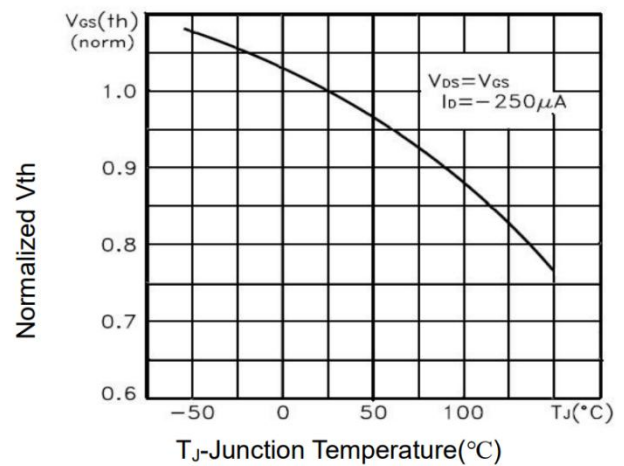
**Figure 7 Capacitance vs Vds**



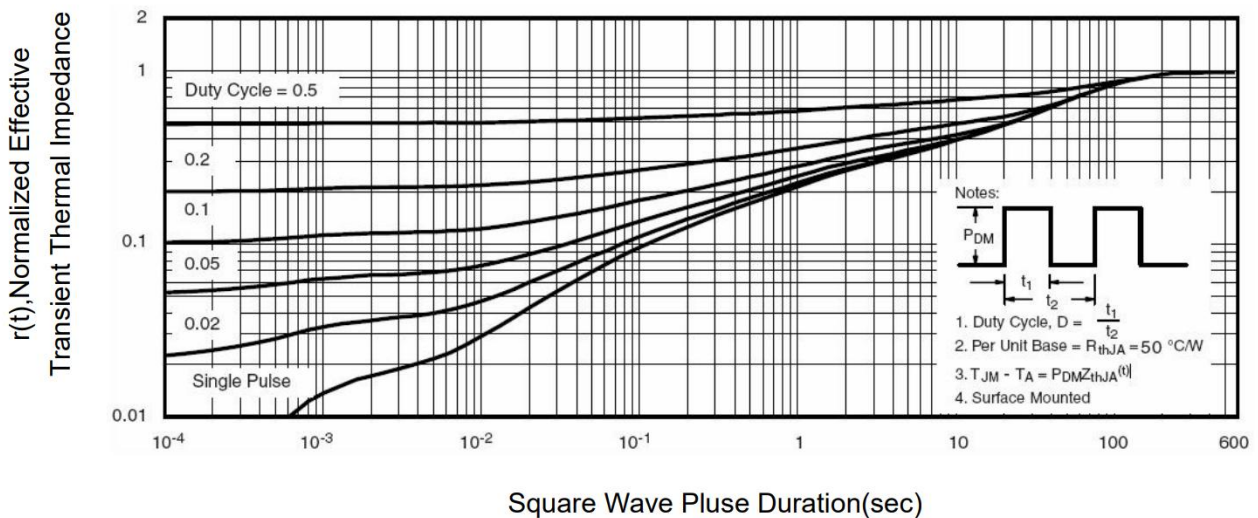
**Figure 8 BV<sub>DSS</sub> vs Junction Temperature**



**Figure 9 Safe Operation Area**

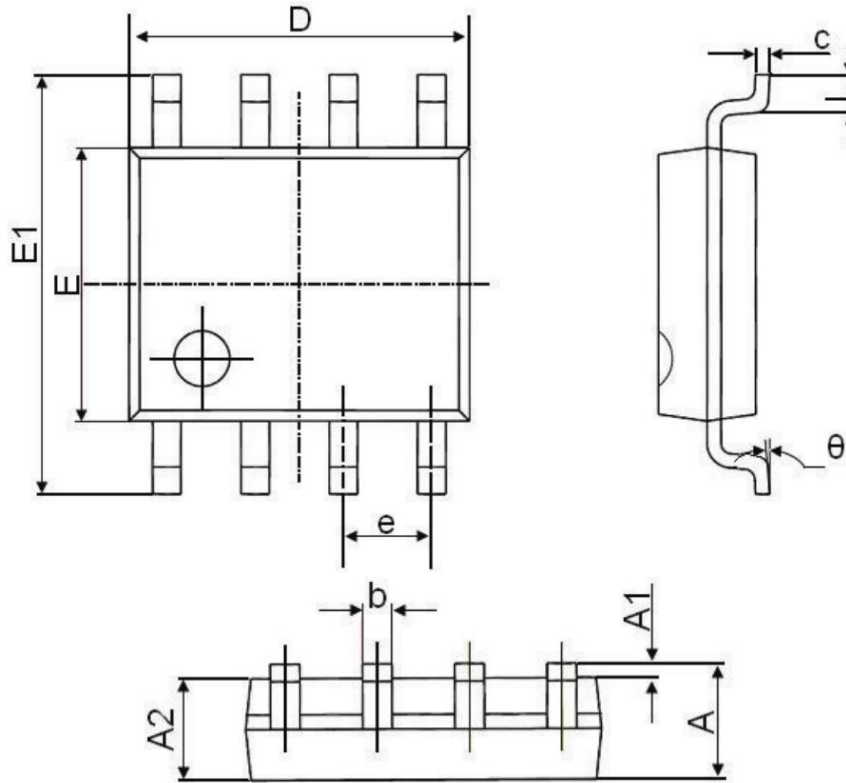


**Figure 10 V<sub>GS(th)</sub> vs Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

### SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°