

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-60V	25mΩ@-10V	-40A
	30mΩ@-4.5V	

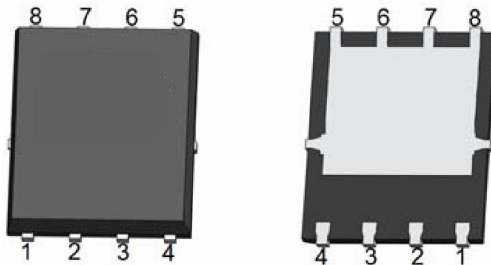
Feature

- High density cell design for low Rdson
- Split gate trench MOSFET technology
- Excellent stability and uniformity
- Extremely low switching loss
- Suffix“-Q1”for AEC-Q101

Application

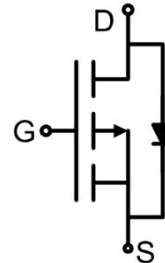
- Load switch
- Industrial DC/DC conversion circuits

Package

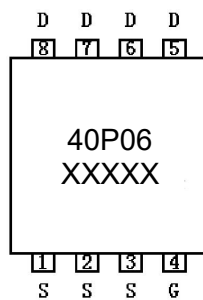


DFN5X6-8L

Circuit diagram



Marking



Absolute maximum ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_C = 25^{\circ}\text{C}$)	I_D	-40	A
Continuous Drain Current ($T_C = 100^{\circ}\text{C}$)	I_D	-25	A
Pulsed Drain Current	I_{DM}	-160	A
Power Dissipation ($T_C = 25^{\circ}\text{C}$)	P_D	88	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	50	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.42	$^{\circ}\text{C}/\text{W}$
Single pulse avalanche energy	E_{AS}	256	mJ
Junction Temperature	T_J	150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Electrical characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-60			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -60\text{V}, V_{GS} = 0\text{V}$			-1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1.3		-2.5	V
Drain-source on-resistance ¹⁾	$R_{DS(on)}$	$V_{GS} = -10\text{V}, I_D = -20\text{A}$		16	25	$\text{m}\Omega$
		$V_{GS} = -4.5\text{V}, I_D = -10\text{A}$		23	30	$\text{m}\Omega$
Gate resistance	R_G	$F = 1.0\text{MHz}$		6		Ω
Dynamic characteristics²⁾						
Input Capacitance	C_{iss}	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		2200		pF
Output Capacitance	C_{oss}			700		
Reverse Transfer Capacitance	C_{rss}			56		
Total Gate Charge	Q_g	$V_{DS} = -30\text{V}, V_{GS} = -10\text{V}, I_D = -20\text{A}$		37.5		nC
Gate-Source Charge	Q_{gs}			8.8		
Gate-Drain Charge	Q_{gd}			7.1		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -30\text{V}, V_{GS} = -10\text{V}, R_L = 2.5\Omega, R_{GEN} = 6\Omega$		9.9		nS
Turn-on rise time	t_r			39.2		
Turn-off delay time	$t_{d(off)}$			72.5		
Turn-off fall time	t_f			64.7		
Source-Drain Diode characteristics						
Diode Forward Current ¹⁾	I_S				-40	A
Diode Forward voltage	V_{SD}	$V_{GS} = 0\text{V}, I_S = -20\text{A}$			-1.3	V
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = -20\text{A}, di/dt = 100\text{A}/\mu\text{s}^1$		33.2		nS
Reverse Recovery Charge	Q_{rr}			22.3		nC

Notes:

- 1) Pulse Test: Pulse Width < 300 μs , Duty Cycle $\leq 2\%$.
- 2) Guaranteed by design, not subject to production testing.

Typical Characteristics

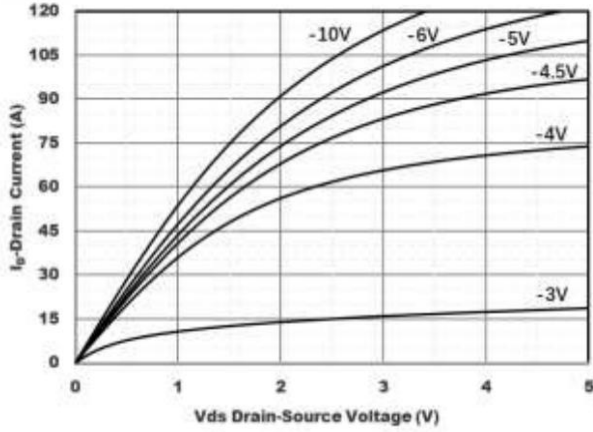


Figure1. Output Characteristics

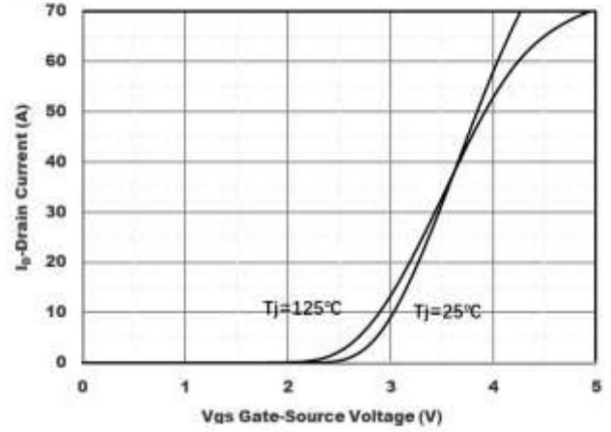


Figure2. Transfer Characteristics

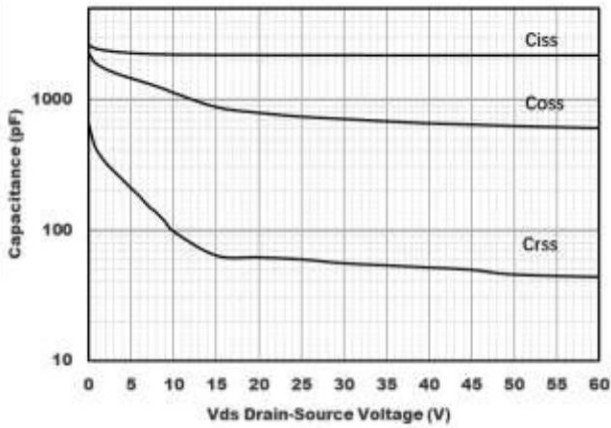


Figure3. Capacitance Characteristics

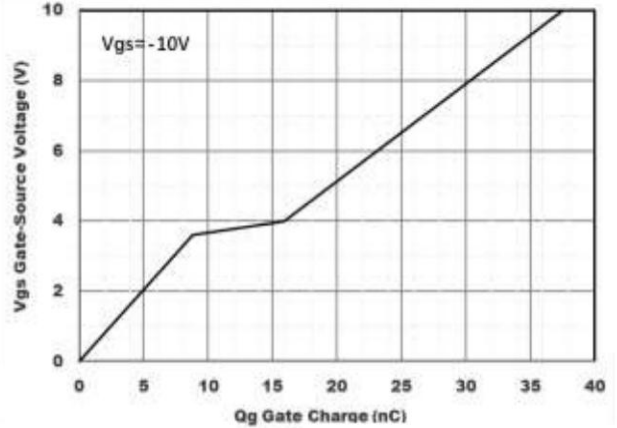


Figure4. Gate Charge

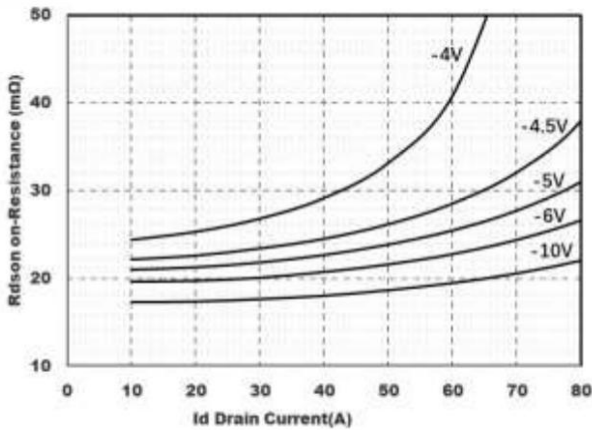


Figure5. : On-Resistance vs. Gate to Source Voltage

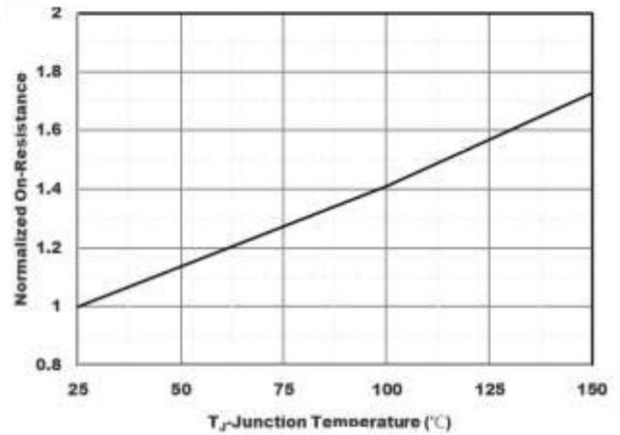


Figure6. Normalized On-Resistance

Typical Characteristics

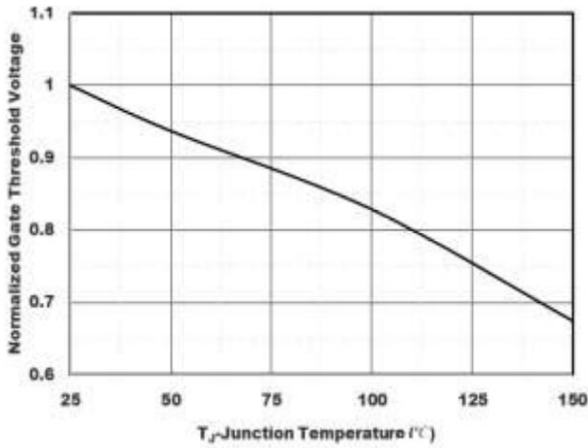


Figure7. Normalized Gate Threshold Voltage

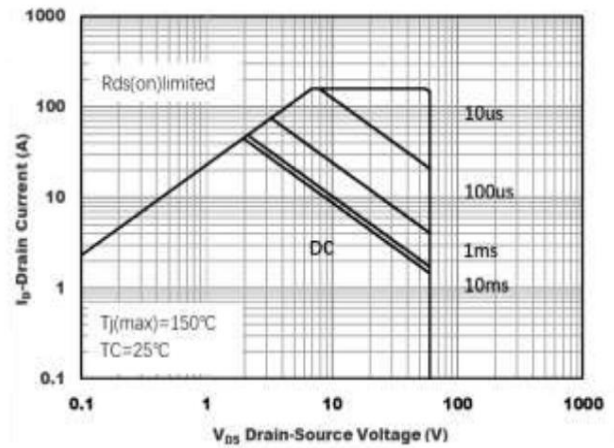


Figure8.Safe Operation Area

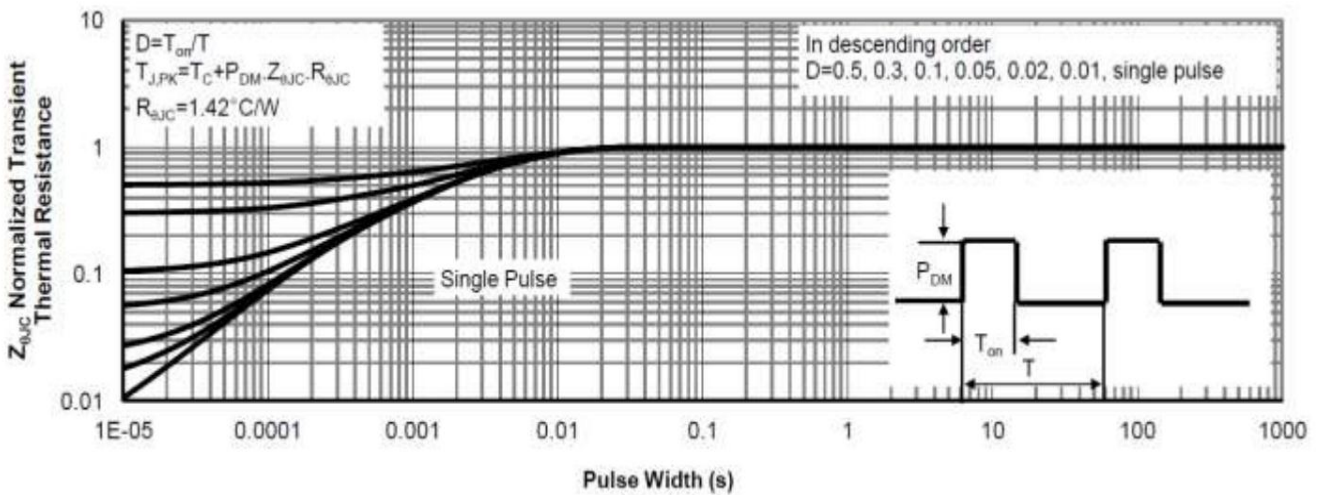
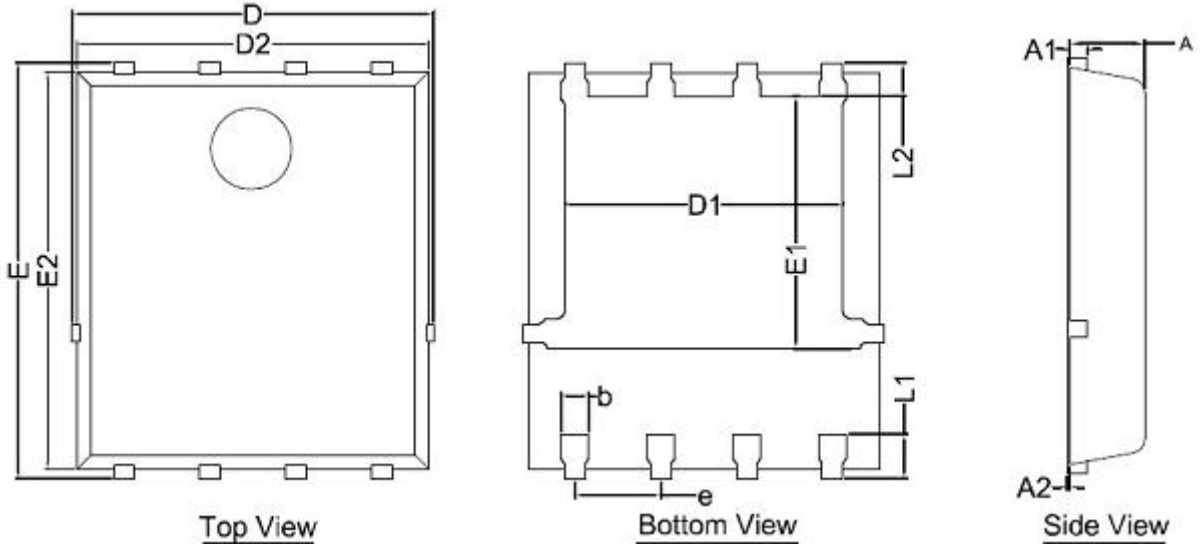


Figure9.Normalized Maximum Transient thermal impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.000	1.200	0.039	0.047
A1	0.254BSC.		0.010BSC.	
A2	0.000	0.100		0.004
D	5.150	5.550	0.202	0.219
E	5.950	6.350	0.234	0.250
D1	3.920	4.320	0.154	0.170
E1	3.520	3.920	0.139	0.154
D2	5.000	5.400	0.197	0.212
E2	5.660	6.060	0.223	0.239
b	0.310	0.510	0.012	0.020
e	1.270BSC.		0.050BSC	
L1	0.560	0.760	0.022	0.030
L2	0.500BSC.		0.020BSC	