AS40P04S-Q1

P-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-40V	14mΩ@-10V	-40A
	20mΩ@-4.5V	

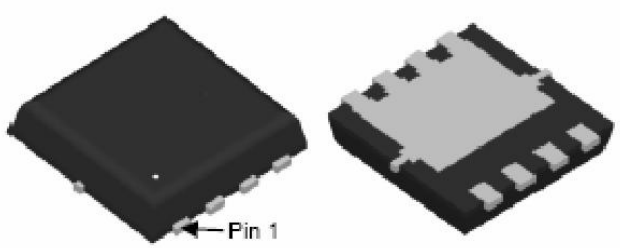
Feature

- High density cell design for ultra low Rdson
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Suffix "-Q1" for AEC-Q101

Application

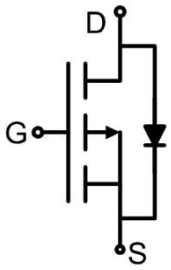
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Package

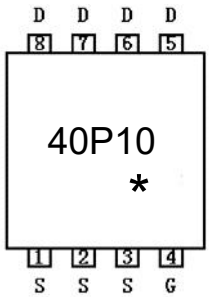


DFN3.3X3.3-8L

Circuit diagram



Marking



Absolute maximum ratings (Ta=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	-40	A
Pulsed Drain Current	I_{DM}	-160	A
Power Dissipation	P_D	3.5	W
Thermal Resistance,Junction-to-Ambient	$R_{\theta JA}$	35.7	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_A=25 °C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-40			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-40V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-1.0	-1.6	-2.5	V
Drain-source on-resistance[1]	$R_{DS(on)}$	V_{GS} =-10V, I_D =-12A		10.5	14	mΩ
		V_{GS} =-4.5V, I_D =-10A		14	20	
Dynamic characteristics[2]						
Input Capacitance	C_{iss}	V_{DS} =-15V,V_{GS} =0V,f =1MHz		3580		pF
Output Capacitance	C_{oss}			323		
Reverse Transfer Capacitance	C_{rss}			220		
Total Gate Charge	Q_g	V_{DS} =-20V,V_{GS} =-10V, ID =-25A		41		nC
Gate-Source Charge	Q_{gs}			11		
Gate-Drain Charge	Q_{gd}			8		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-20V,V_{GS}=-10V, I_D =-1A,R_G=6Ω		12		nS
Turn-on rise time	t_r			25		
Turn-off delay time	$t_{d(off)}$			30		
Turn-off fall time	t_f			24		
Source-Drain Diode characteristics						
Diode Forward voltage	V_{SD}	V_{GS} =0V, I_S=-1A			-1.2	V

Notes:

1) Pulse Test: Pulse Width < 300μs, Duty Cycle ≤2%.

2) Guaranteed by design, not subject to production testing.

Typical Characteristics

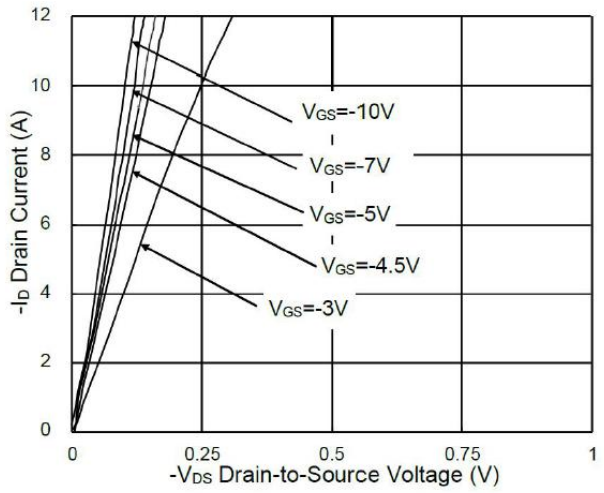


Fig.1 Typical Output Characteristics

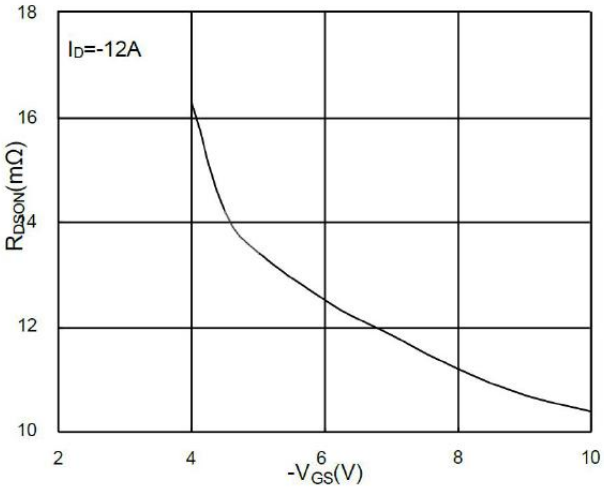


Fig.2 On-Resistance v.s Gate-Source

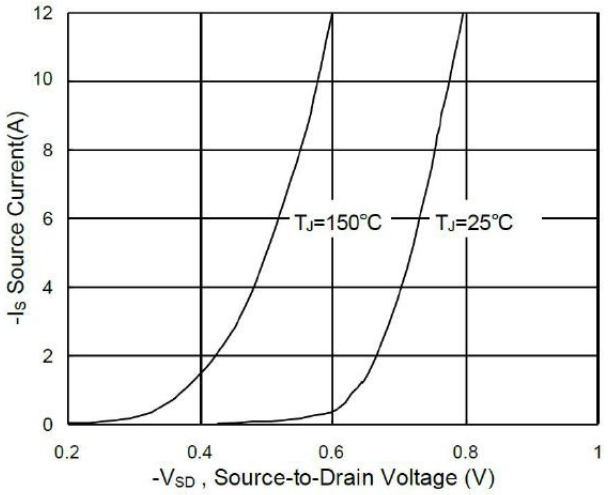


Fig.3 Forward Characteristics Of Reverse

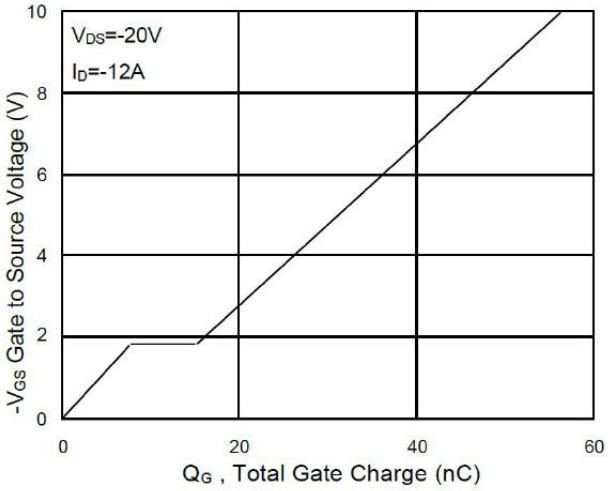


Fig.4 Gate-Charge Characteristics

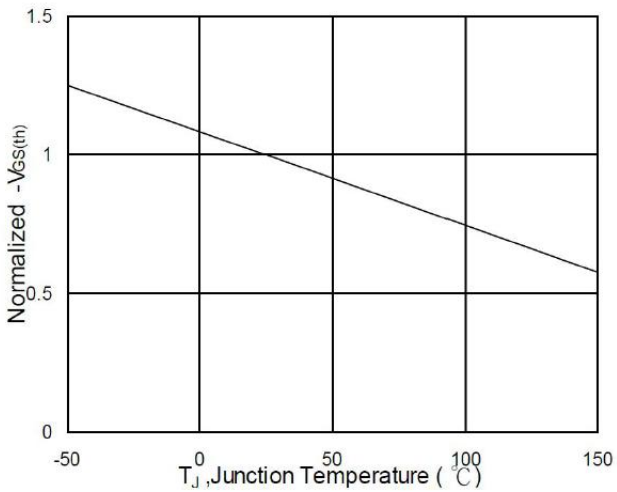


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

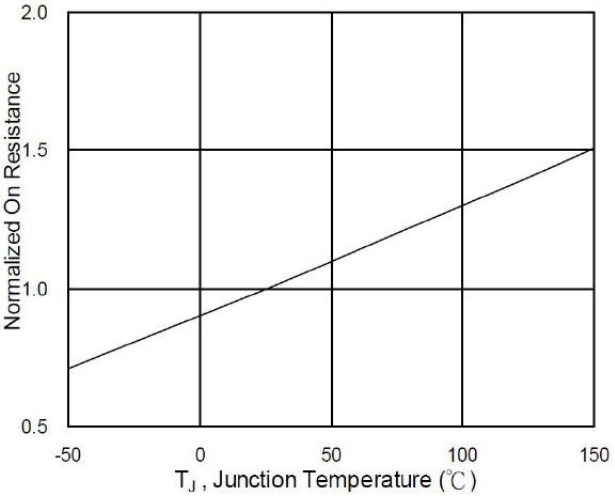


Fig.6 Normalized R_{DSON} v.s T_J

Typical Characteristics

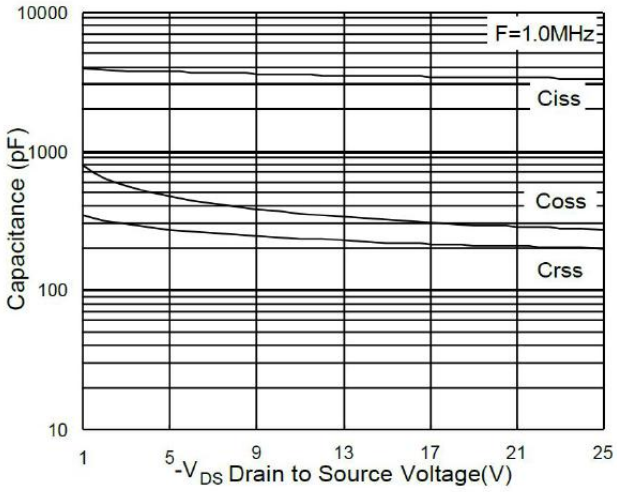


Fig.7 Capacitance

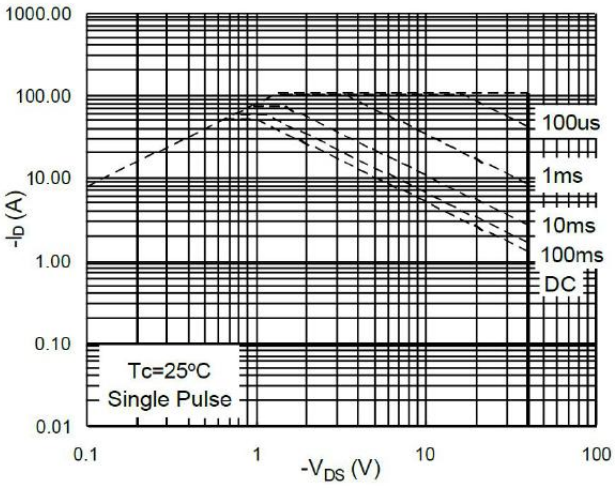


Fig.8 Safe Operating Area

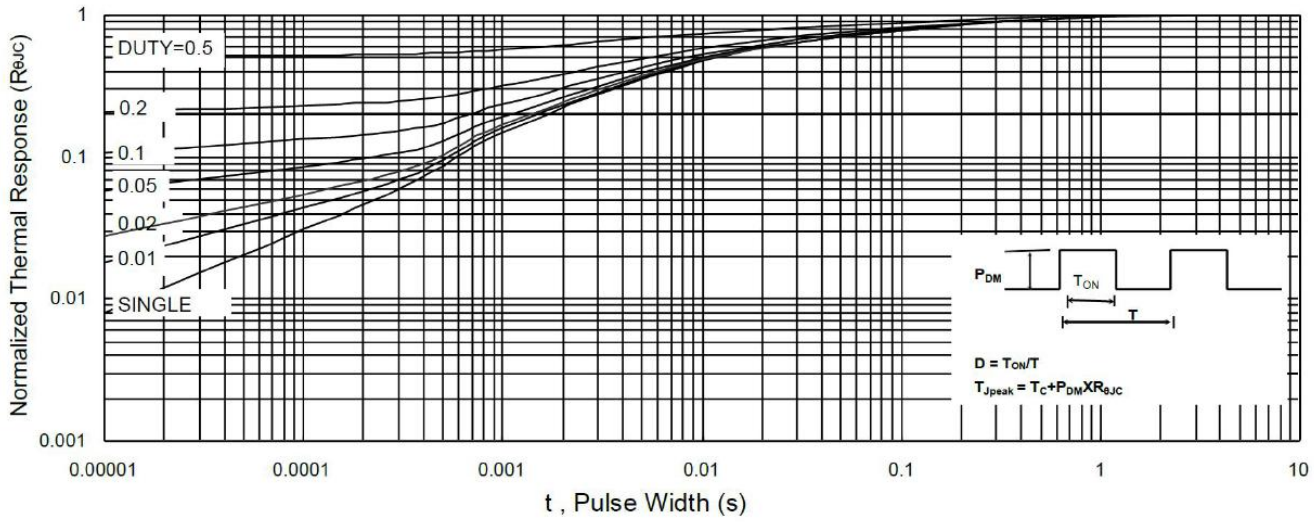


Fig.9 Normalized Maximum Transient Thermal Impedance

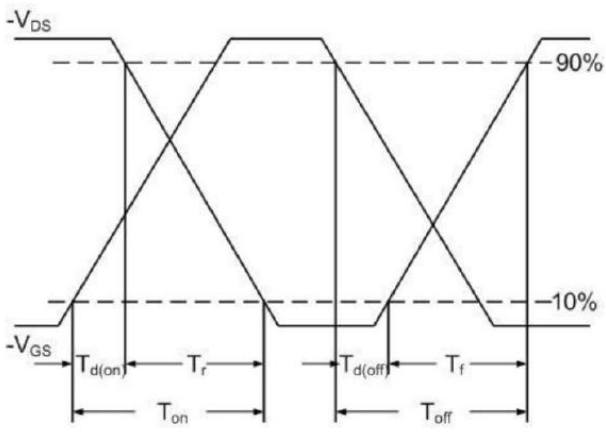


Fig.10 Switching Time Waveform

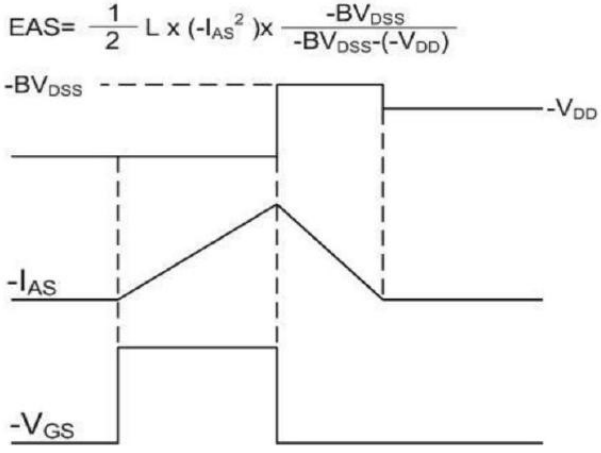
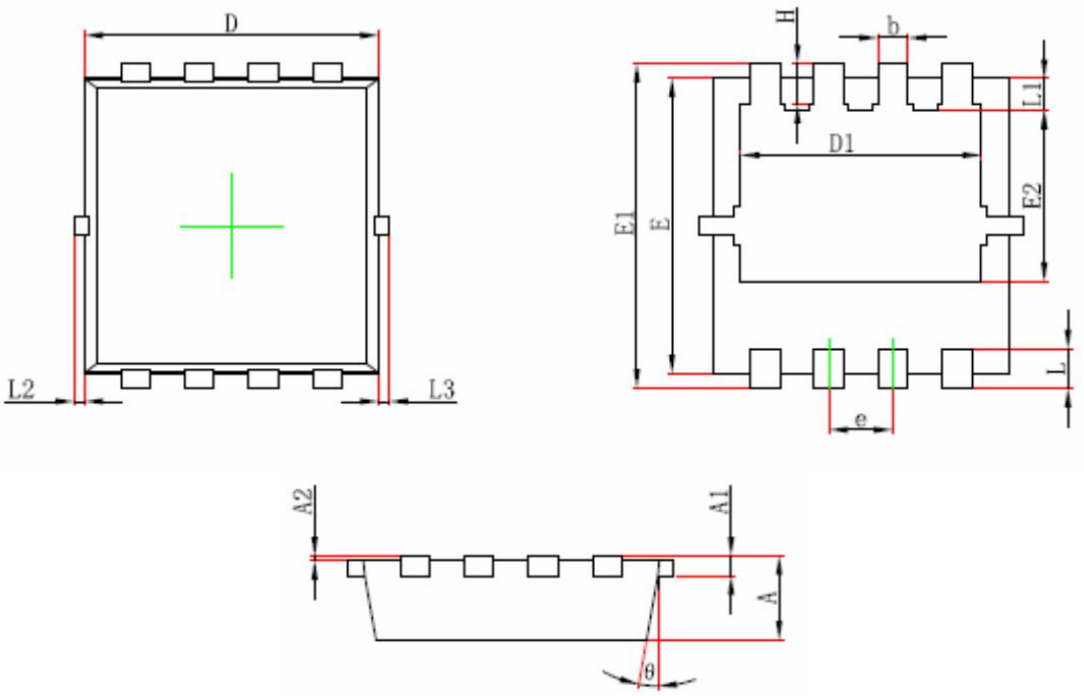


Fig.11 Unclamped Inductive Waveform

DFN3.3X3.3-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF		0.006 REF	
A2	0.000	0.050	0.000	0.002
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0.000	0.100	0.000	0.004
L3	0.000	0.100	0.000	0.004
H	0.315	0.515	0.012	0.020
θ	9 °	13 °	9 °	13 °