

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
30V	25mΩ@10V	5.6A
	31mΩ@4.5V	
	45mΩ@2.5V	

Feature

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Suffix "-Q1" for AEC-Q101

Application

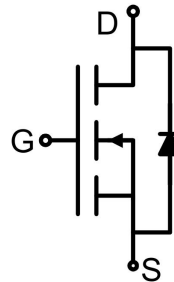
- Load Switch for Portable Devices
- Battery protection
- Power management

Package

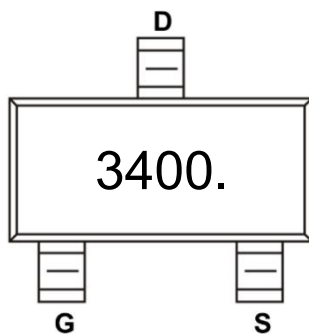


SOT-23

Circuit diagram



Marking



Absolute maximum ratings (Ta=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±12	V
Continuous Drain Current	I _D	5.6	A
Pulsed Drain Current	I _{DM}	23	A
Power Dissipation	P _D	1.2	W
Thermal Resistance, Junction-to-Ambient ³⁾	R _{θJA}	104	°C/W
Junction Temperature	T _J	150	°C
Storage Temperature	T _{STG}	-55 ~ +150	°C

Electrical characteristics (T_A=25 °C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
Gate-body leakage current	I _{GSS}	V _{GS} = ±12V, V _{DS} = 0V			±100	nA
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.65	0.9	1.5	V
Drain-source on-resistance ¹⁾	R _{DS(on)}	V _{GS} = 10V, I _D = 5.6A		20	27	mΩ
		V _{GS} = 4.5V, I _D = 5.0A		23	31	
		V _{GS} = 2.5V, I _D = 3.0A		27	45	
Dynamic characteristics²⁾						
Input Capacitance	C _{iss}	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz		630		pF
Output Capacitance	C _{oss}			55		
Reverse Transfer Capacitance	C _{rss}			71		
Total Gate Charge	Q _g	V _{DS} = 15V, V _{GS} = 10V, I _D = 5.6A		17.3		nC
Gate-Source Charge	Q _{gs}			2.1		
Gate-Drain Charge	Q _{gd}			2		
Turn-on delay time	t _{d(on)}	V _{DD} = 15V, V _{GS} = 10V, I _D = 5.6A R _{GEN} = 3Ω		4.4		nS
Turn-on rise time	t _r			28.2		
Turn-off delay time	t _{d(off)}			16.2		
Turn-off fall time	t _f			26		
Source-Drain Diode characteristics						
Diode Forward Current ¹⁾	I _S				5.6	A
Diode Forward voltage	V _{DS}	V _{GS} = 0V, I _S = 5.6A			1.2	V

Notes:

- 1) Pulse Test: Pulse Width < 300μs, Duty Cycle ≤ 2%.
- 2) Guaranteed by design, not subject to production testing.
- 3) R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

Typical Characteristics

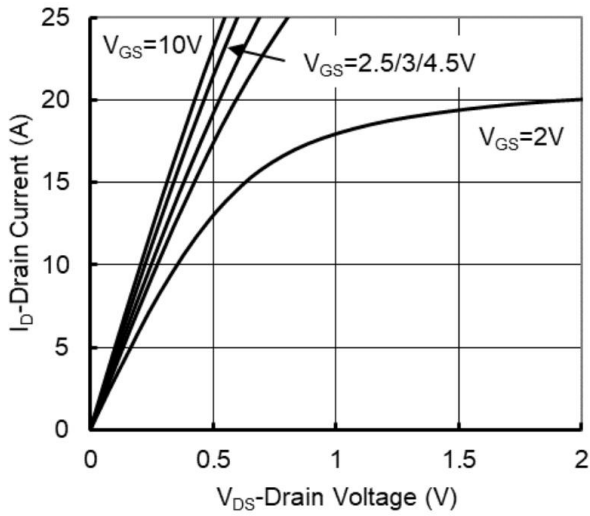


Figure1. Output Characteristics

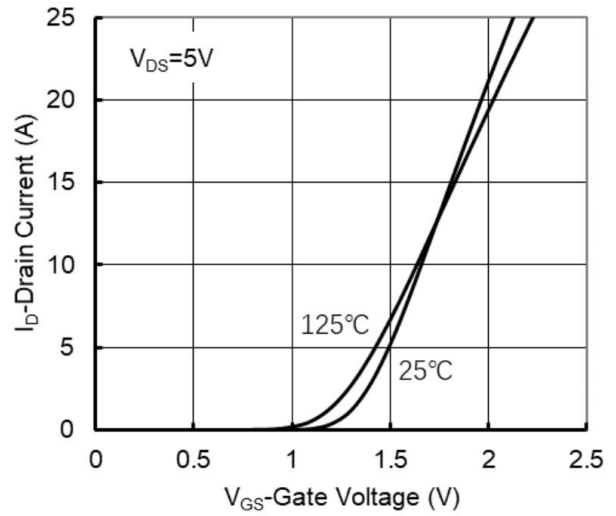


Figure2. Transfer Characteristics

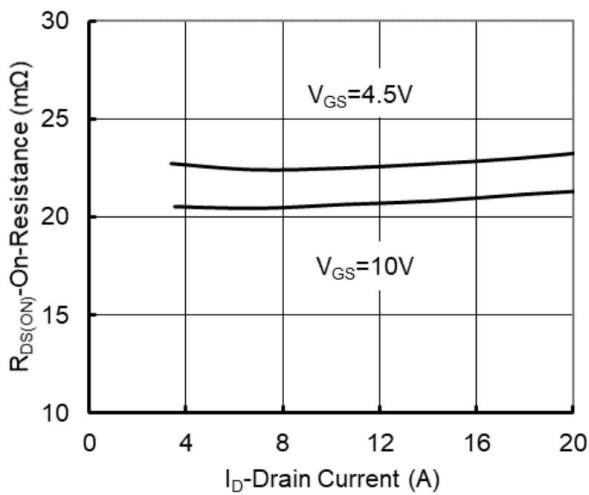


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

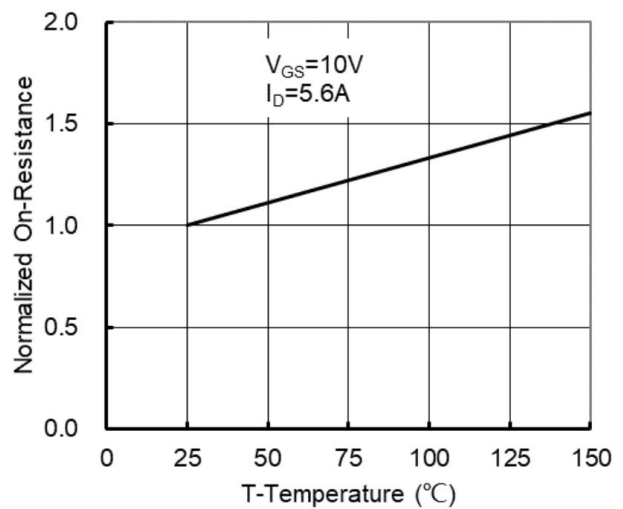


Figure 4: On-Resistance vs. Junction Temperature

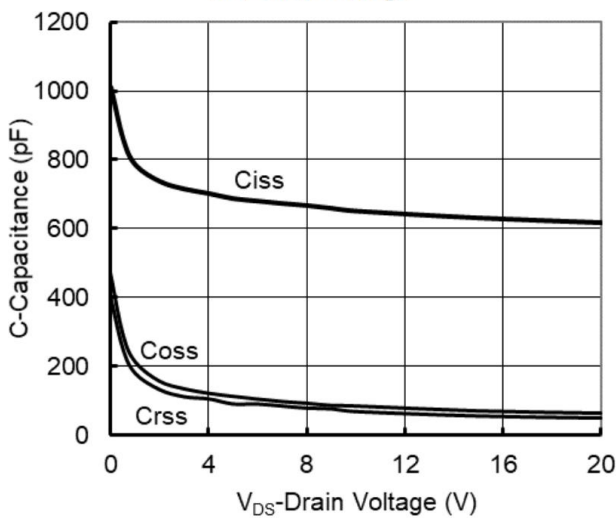


Figure5. Capacitance Characteristics

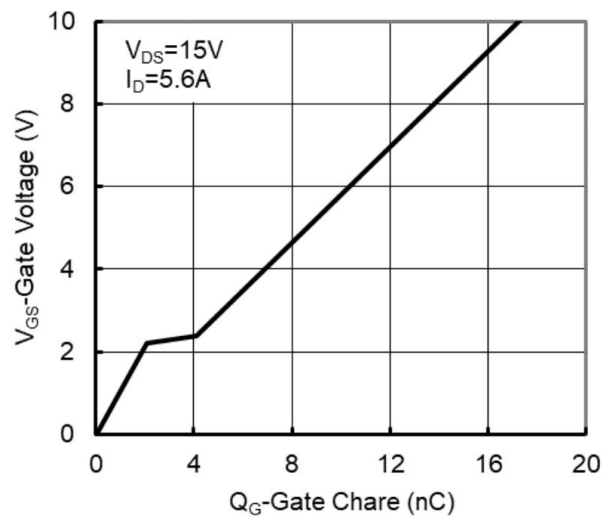


Figure6. Gate Charge

Typical Characteristics

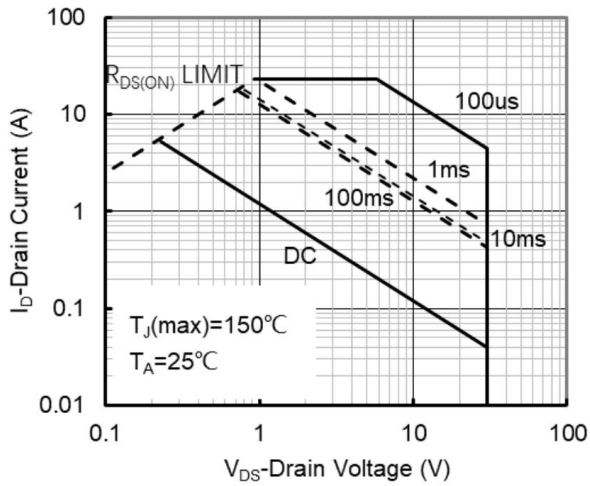


Figure 7. Safe Operation Area

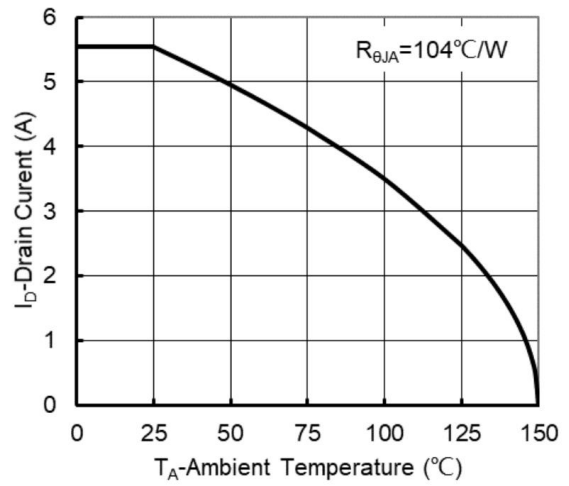


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

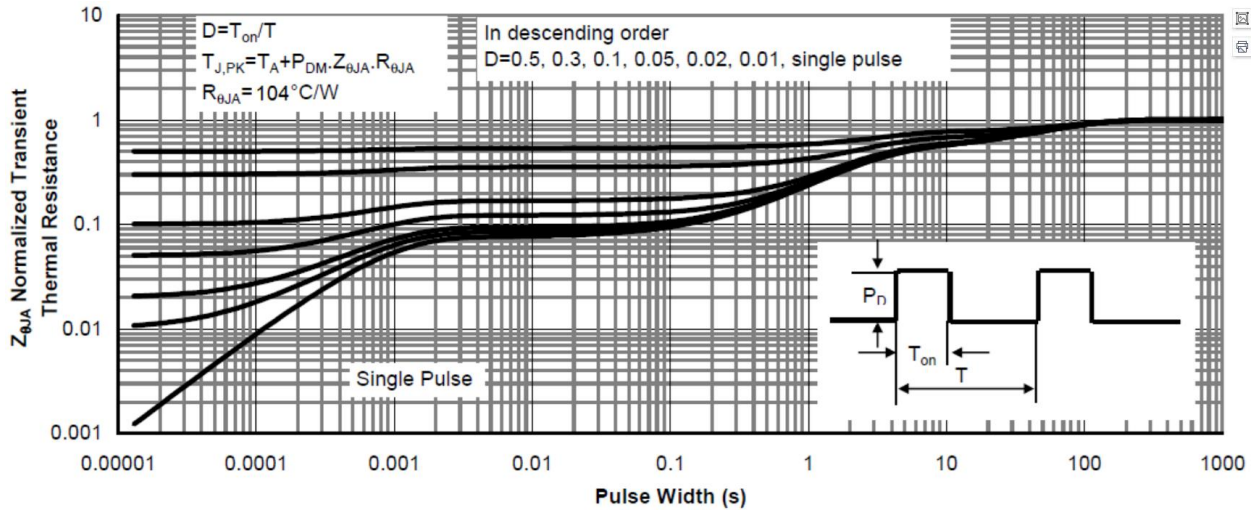
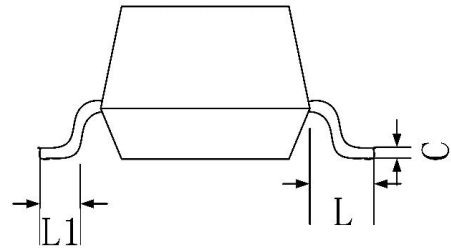
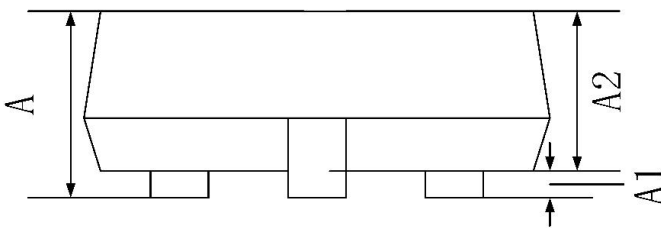
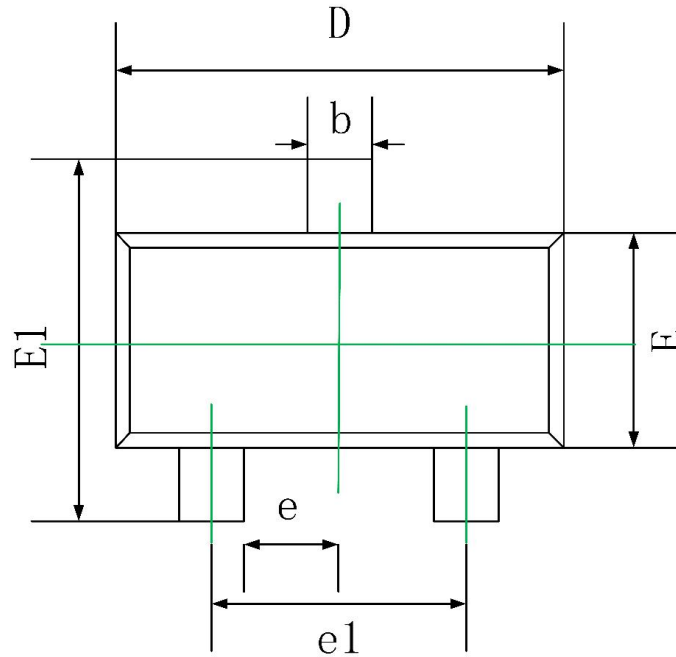


Figure 9. Normalized Maximum Transient Thermal Impedance

SOT-23 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020