AS2305-Q1

P-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-20V	42mΩ@-4.5V	-5.4A
	55mΩ@-2.5V	
	75mΩ@-1.8V	

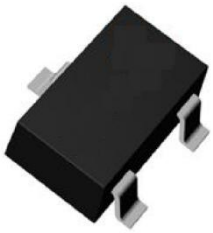
Feature

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Suffix"-Q1"for AEC-Q101

Application

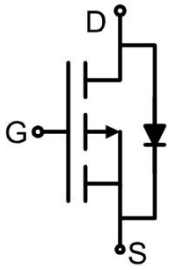
- Load Switch for Portable Devices
- DC/DC Converter
- Power management

Package

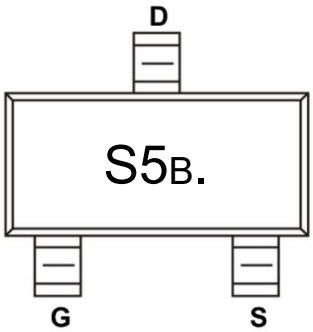


SOT-23

Circuit diagram



Marking



AS2305-Q1

P-Channel Enhancement Mode MOSFET

Absolute maximum ratings (Ta=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	-5.4	A
Pulsed Drain Current	I_{DM}	-22	A
Power Dissipation	P_D	1.2	W
Thermal Resistance Junction-to-Ambient 3)	$R_{\theta JA}$	104	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_A=25 °C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}= 0V, I_D =-250μA	-20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-20V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±10V, V_{DS} = 0V			±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.4	-0.62	-1.0	V
Drain-source on-resistance1)	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-5.4A		27	42	mΩ
		V_{GS} =-2.5V, I_D =-4.0A		36	55	
		V_{GS} =-1.8V, I_D =-3.0A		48	75	
Dynamic characteristics2)						
Input Capacitance	C_{iss}	V_{DS} =-10V,V_{GS} =0V,f =1MHz		1010		pF
Output Capacitance	C_{oss}			130		
Reverse Transfer Capacitance	C_{rss}			109		
Total Gate Charge	Q_g	V_{DS} =-10V,V_{GS} =-4.5V, I_D =-4A		11		nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			2.54		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-10V, V_{GS} =-4.5V, R_{GEN}=3Ω, R_L=2.5Ω		8.4		nS
Turn-on rise time	t_r			36.2		
Turn-off delay time	$t_{d(off)}$			76.8		
Turn-off fall time	t_f			56.2		
Source-Drain Diode characteristics						
Diode Forward Current1)	I_S				-5.4	A
Diode Forward voltage	V_{DS}	V_{GS} =0V, I_S=-5.4A			-1.2	V

Notes:

1) Pulse Test: Pulse Width < 300μs, Duty Cycle ≤2%.

2) Guaranteed by design, not subject to production testing.

3) $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

Typical Characteristics

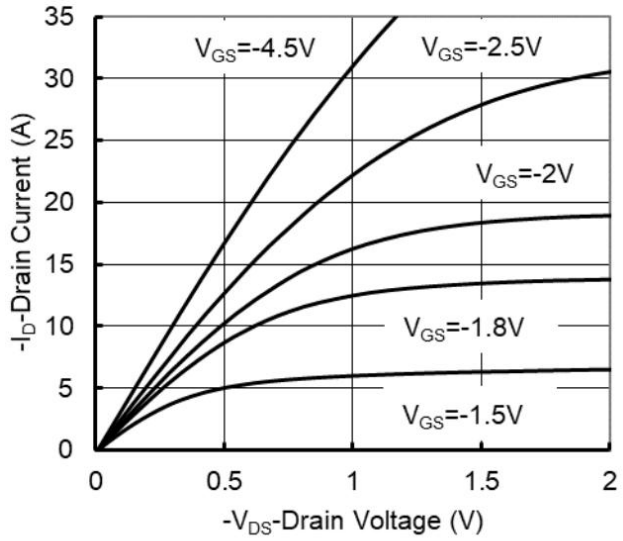


Figure1. Output Characteristics

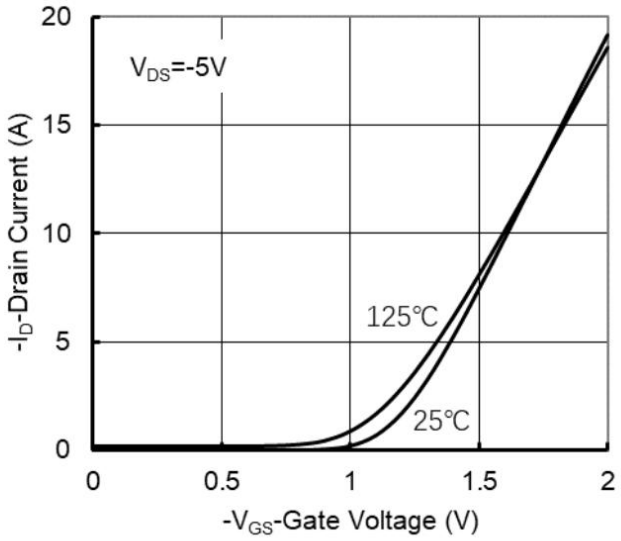


Figure2. Transfer Characteristics

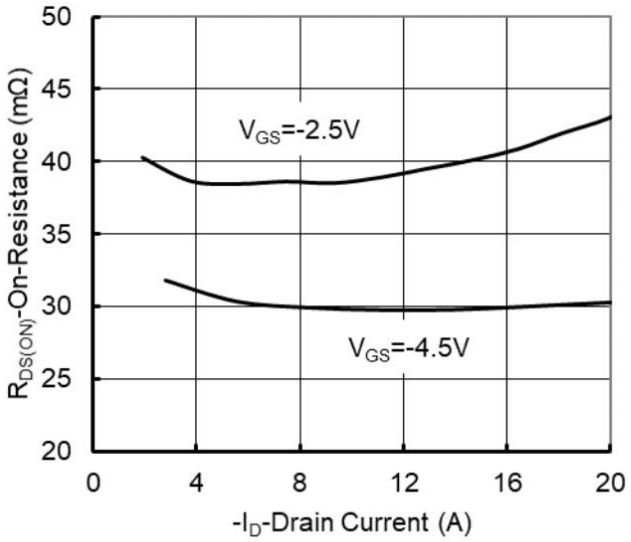


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

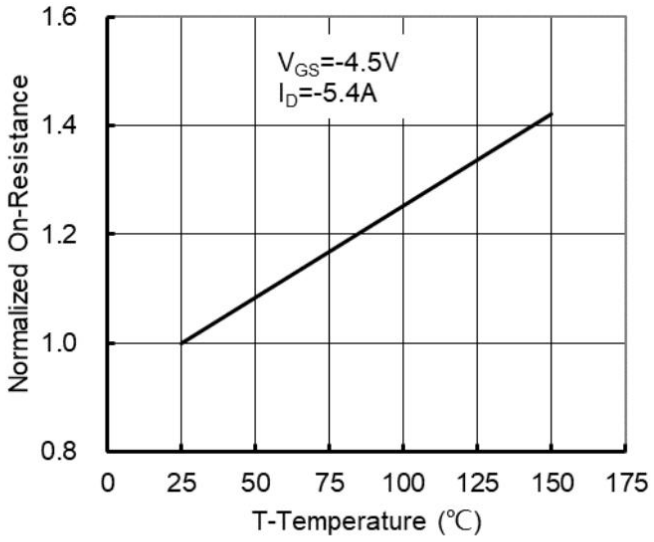


Figure 4: On-Resistance vs. Junction Temperature

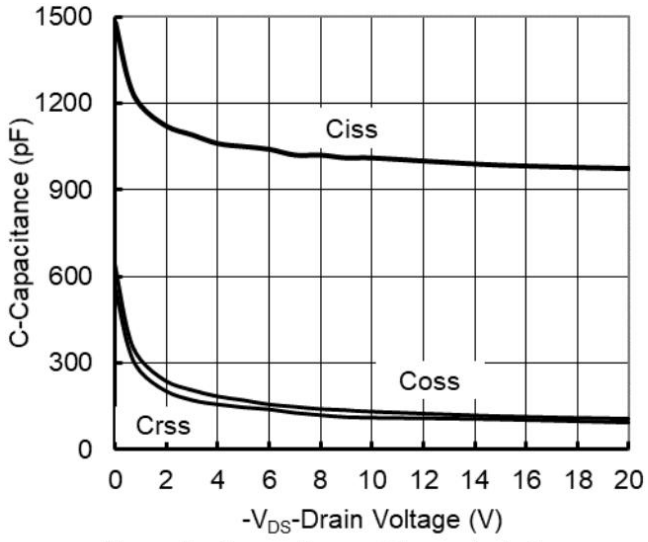


Figure5. Capacitance Characteristics

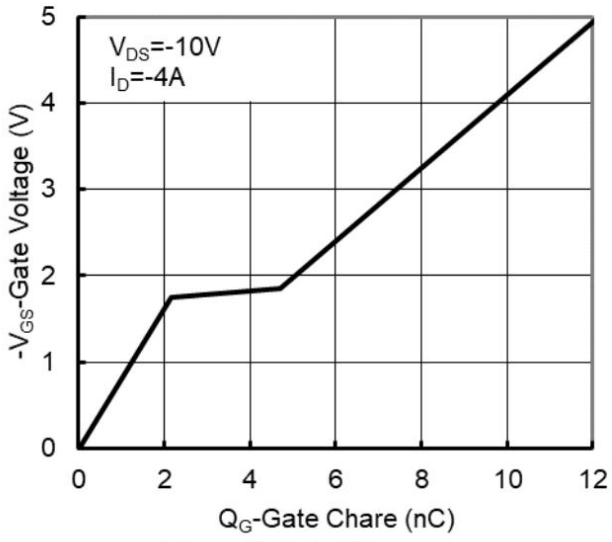


Figure6. Gate Charge

Document ID	Issued Date	Revised Date	Revision	Page.
AS-1150171	2003/03/08	2015/05/16	D	5

Typical Characteristics

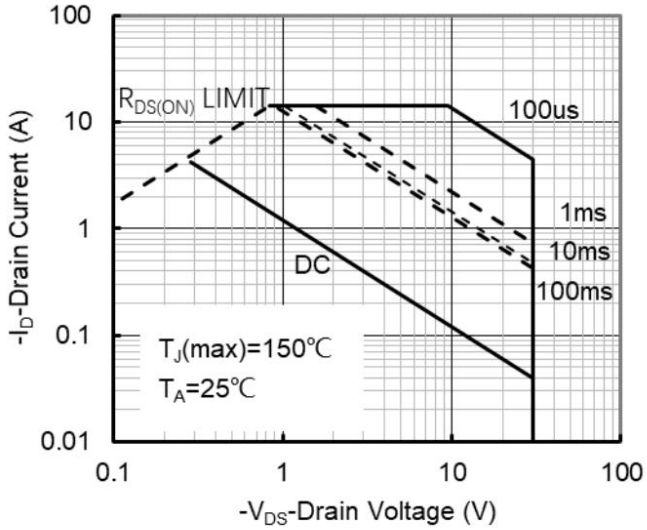


Figure7. Safe Operation Area

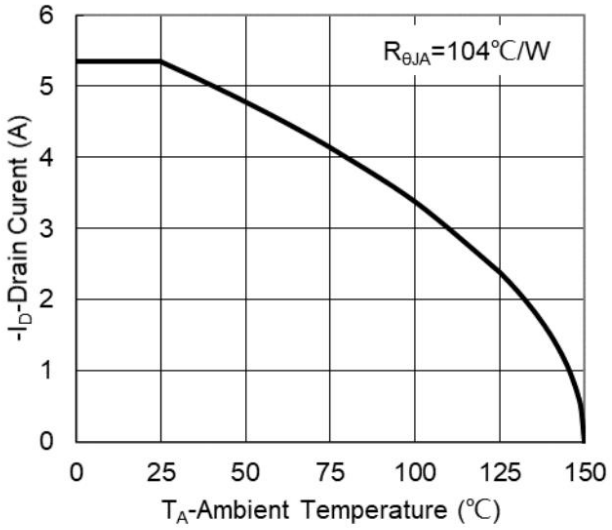


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

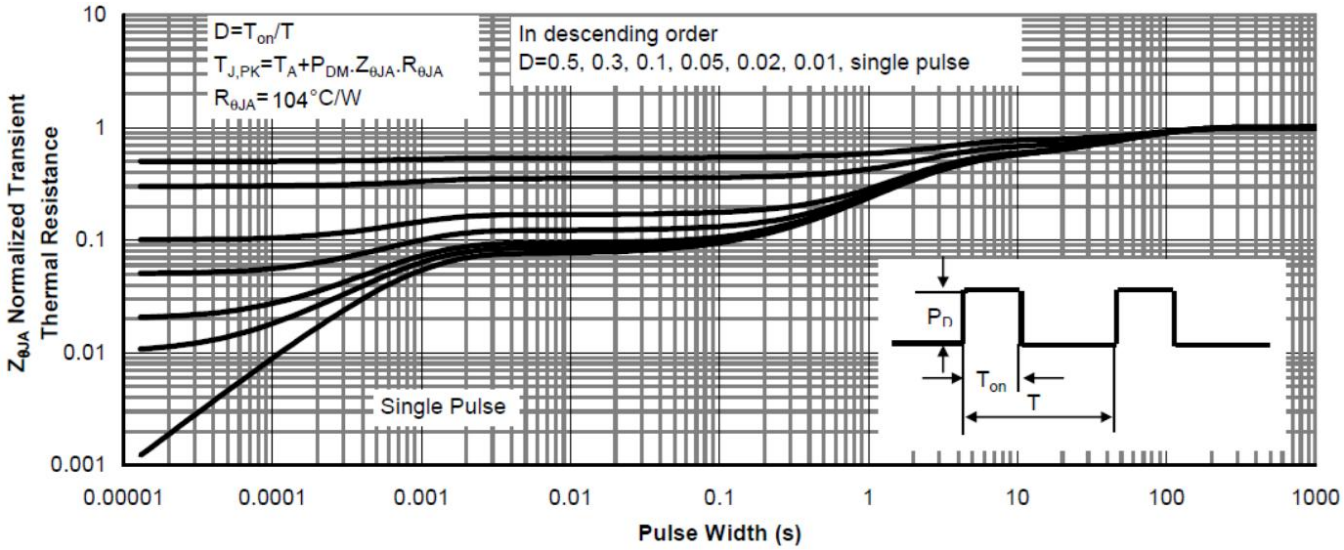
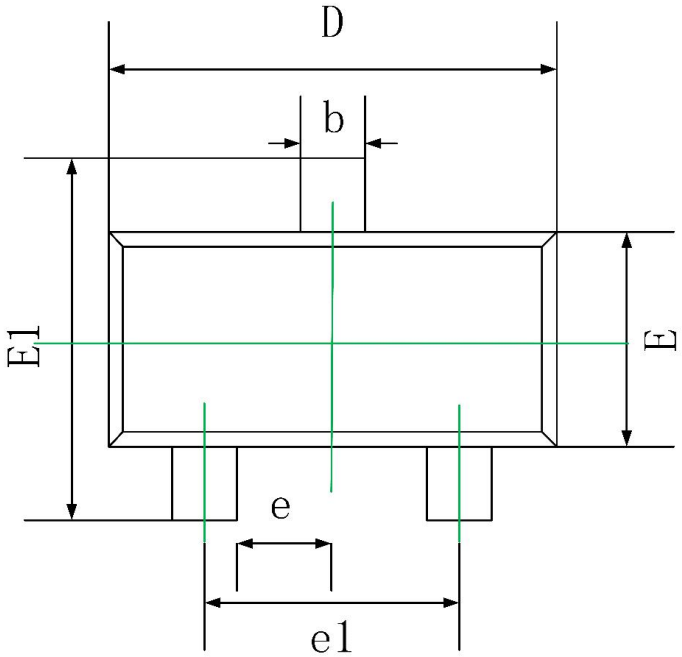
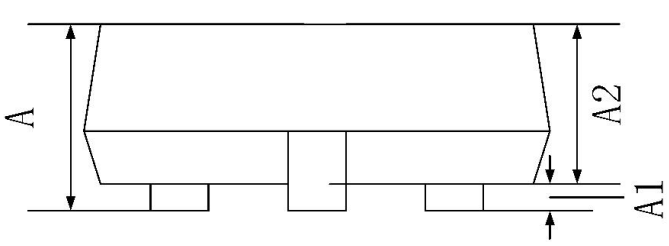
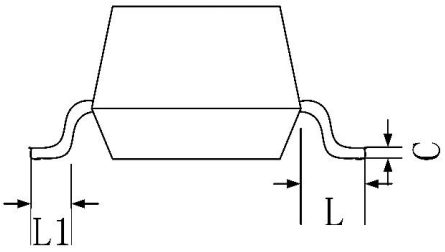


Figure9. Normalized Maximum Transient Thermal Impedance

SOT-23 Package Information







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.200	0.003	0.008
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020