AS06P06S-Q1

P-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-60V	47mΩ@-10V	-5.9A
	60mΩ@-4.5V	

Feature

- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance
- Suffix "-Q1" for AEC-Q101

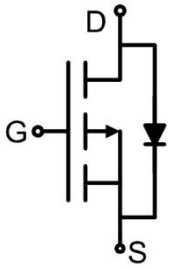
Application

- Load Switch
- Battery Protection

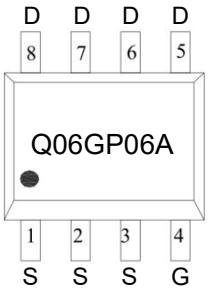
Package

SOP-8

Circuit diagram



Marking



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Absolute maximum ratings (Ta=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	-5.9	A
Pulsed Drain Current[1)]	I_{DM}	-30	A
Power Dissipation[2)]	P_D	3.1	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	59	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_J=25 ºC, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-60			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-60V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-1.3	-1.8	-2.5	V
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} =-10V, I_D =-6A		35	47	mΩ
		V_{GS} =-4.5V, I_D =-3A		45	60	
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =-30V,V_{GS} =0V,f =1MHz		1100		pF
Output Capacitance	C_{oss}			350		
Reverse Transfer Capacitance	C_{rss}			28		
Total Gate Charge	Q_g	V_{DS} =-30V,V_{GS} =-10V, I_D =-3A		18.7		nC
Gate-Source Charge	Q_{gs}			4.7		
Gate-Drain Charge	Q_{gd}			3.0		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-30V,V_{GS}=-10V, I_D =-3A,R_{GEN}=6Ω		7.5		nS
Turn-on rise time	t_r			39.5		
Turn-off delay time	$t_{d(off)}$			43.6		
Turn-off fall time	t_f			55.1		
Source-Drain Diode characteristics						
Diode Forward Current[1)]	I_S				-6	A
Diode Forward voltage	V_{DS}	V_{GS} =0V, I_S=-6A			-1.3	V

Notes:

1) Repetitive rating; pulse width limited by max. junction temperature.

2) Pd is based on max. junction temperature, using ≤10s junction-ambient thermal resistance.

Typical Characteristics

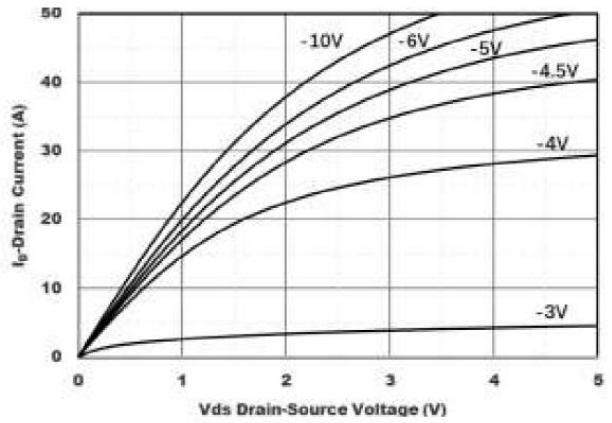


Figure1. Output Characteristics

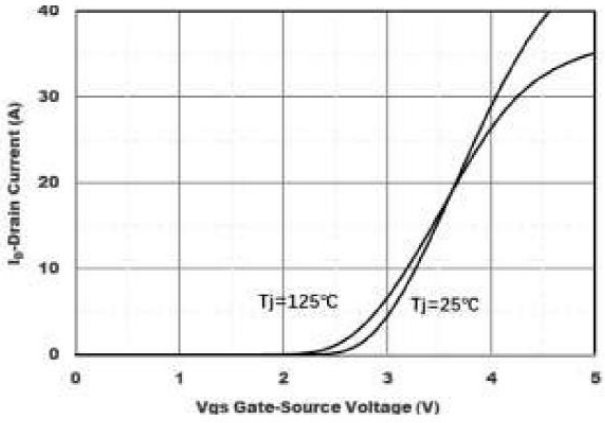


Figure2. Transfer Characteristics

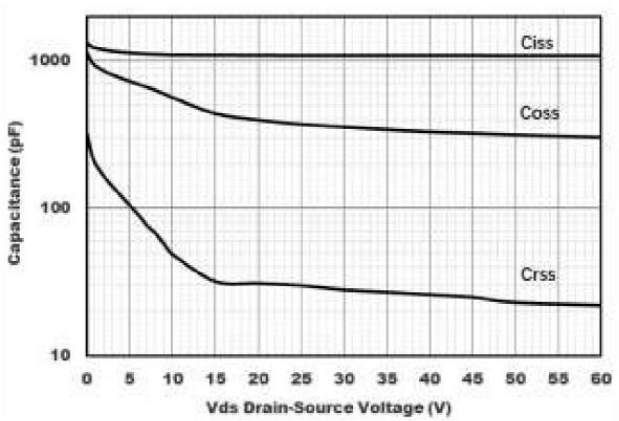


Figure3. Capacitance Characteristics

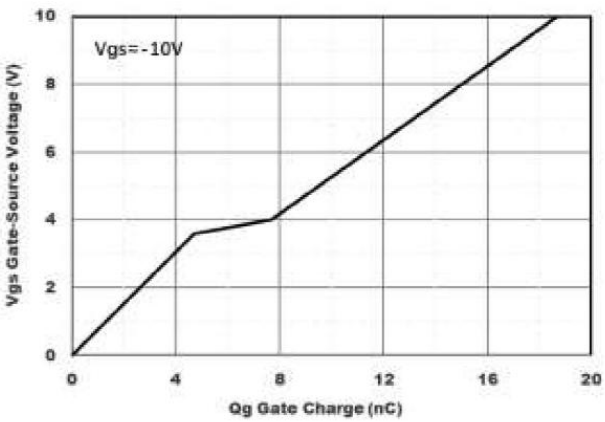


Figure4. Gate Charge

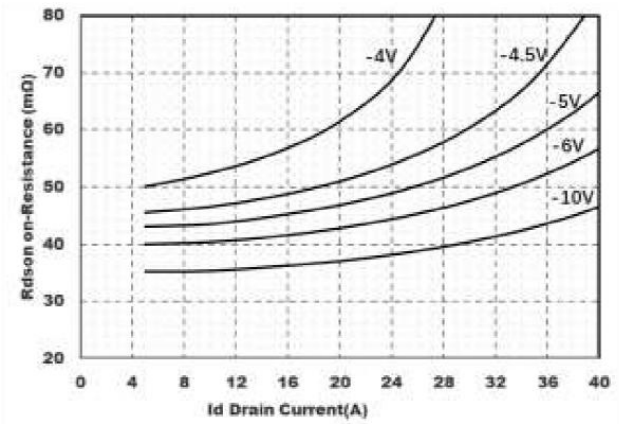


Figure5. : On-Resistance vs. Gate to Source Voltage

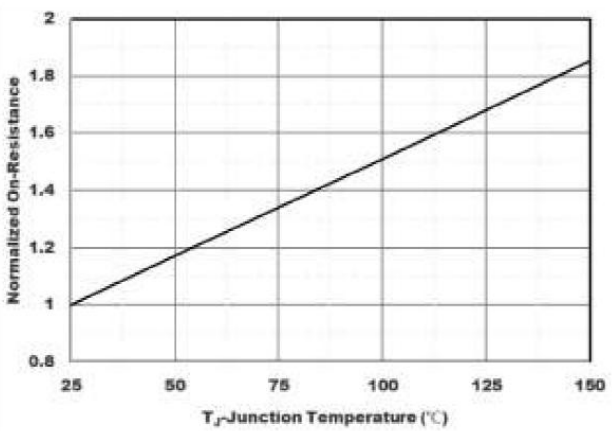


Figure6.Normalized On-Resistance

Typical Characteristics

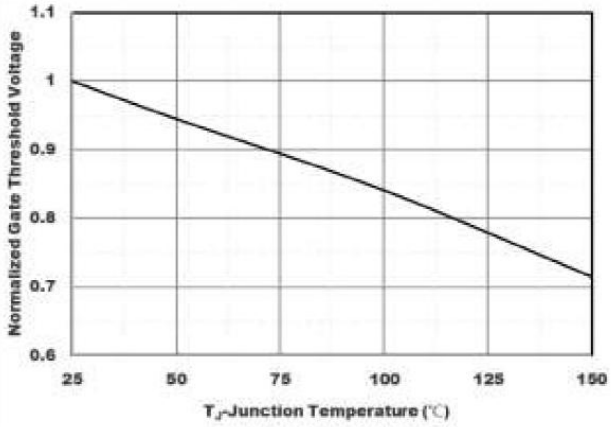


Figure7. Normalized Gate Threshold Voltage

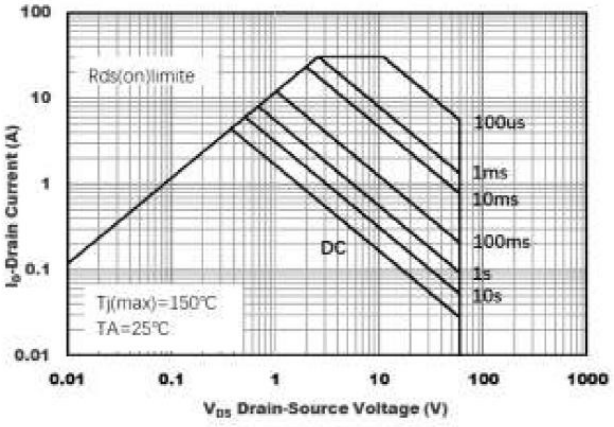


Figure8.Safe Operation Area

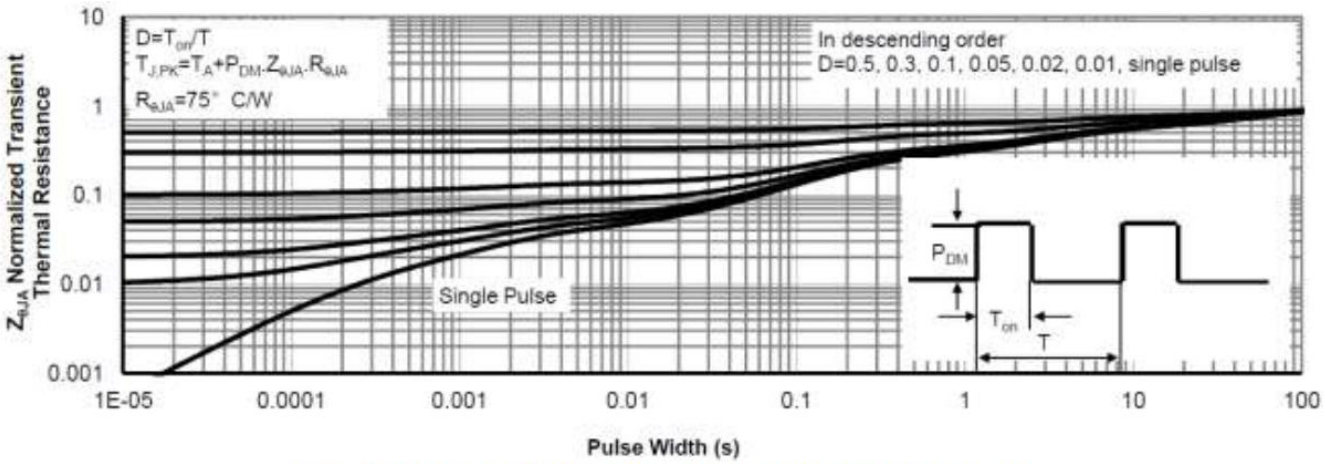
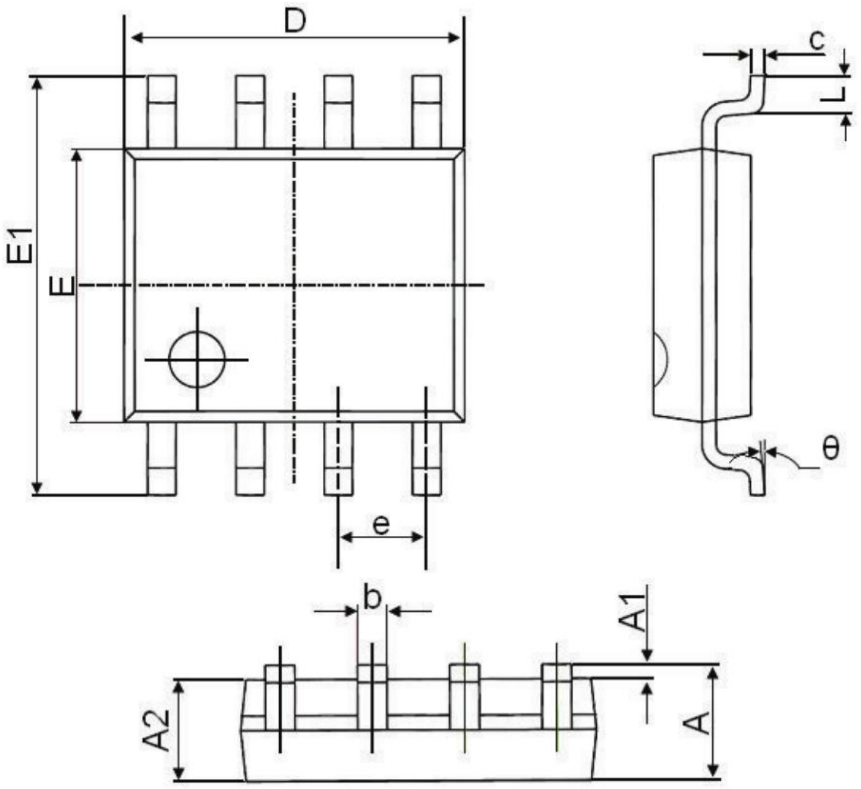


Figure9. Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°