AS0603S-Q1

N-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
60V	100mΩ@10V	3A
	120mΩ@4.5V	

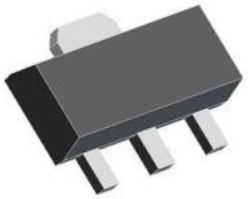
Feature

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Suffix "-Q1" for AEC-Q101

Application

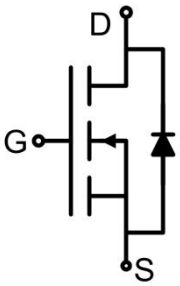
- DC-DC Converters
- Power management functions

Package

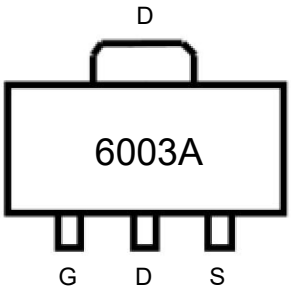


SOT-89

Circuit diagram



Marking



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Absolute maximum ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	3	A
Continuous Drain Current(T_A=70℃)	I_D(T_A=70℃)	2.4	A
Pulsed Drain Current[1)]	I_{DM}	12	A
Power Dissipation	P_D	0.69	W
Thermal Resistance from Junction to Ambient[2)]	$R_{\theta JA}$	180	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}= 0V, I_D =250μA	60			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =60V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1.0	1.3	2.0	V
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} =10V, I_D =3A		86	100	mΩ
		V_{GS} =4.5V, I_D =2A		92	120	
Dynamic characteristics[3)]						
Input Capacitance	C_{iss}	V_{DS} =10V,V_{GS} =0V,f =1MHz		409		pF
Output Capacitance	C_{oss}			50		
Reverse Transfer Capacitance	C_{rss}			41		
Total Gate Charge	Q_g	V_{DS} =30V,V_{GS} =10V,I_D =3A		10.27		nC
Gate-Source Charge	Q_{gs}			1.65		
Gate-Drain Charge	Q_{gd}			2.11		
Turn-on delay time	$t_{d(on)}$	V_{GS}=10V,V_{DS}=30V, R_L=20Ω,R_{GEN}=3Ω		3.6		nS
Turn-on rise time	t_r			17.6		
Turn-off delay time	$t_{d(off)}$			13		
Turn-off fall time	t_f			23		
Source-Drain Diode characteristics						
Diode Forward Current	I_S				3	A
Diode Forward voltage	V_{SD}	V_{GS} =0V, I_S=3A			1.2	V

Notes:

1) Pulse Test: Pulse Width < 300μs, Duty Cycle ≤2%.

2) $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

3) Guaranteed by design, not subject to production testing.

Typical Characteristics

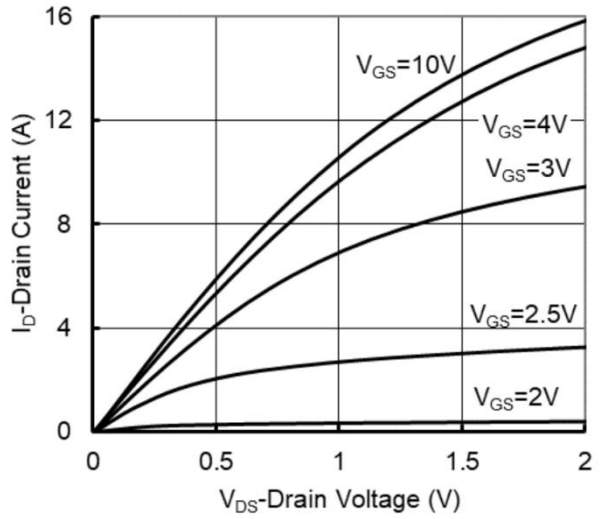


Figure1. Output Characteristics

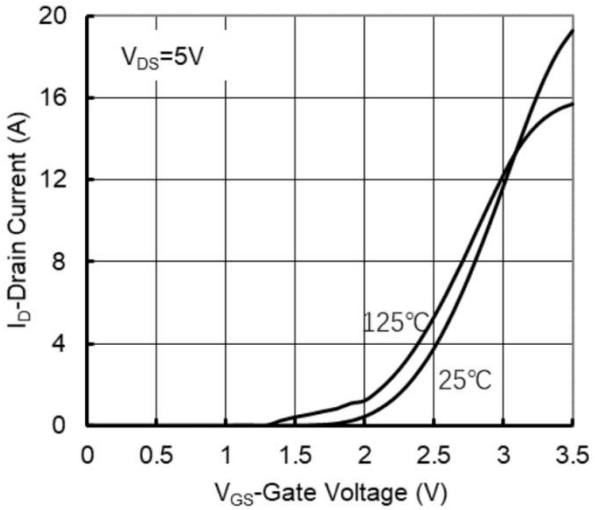


Figure2. Transfer Characteristics

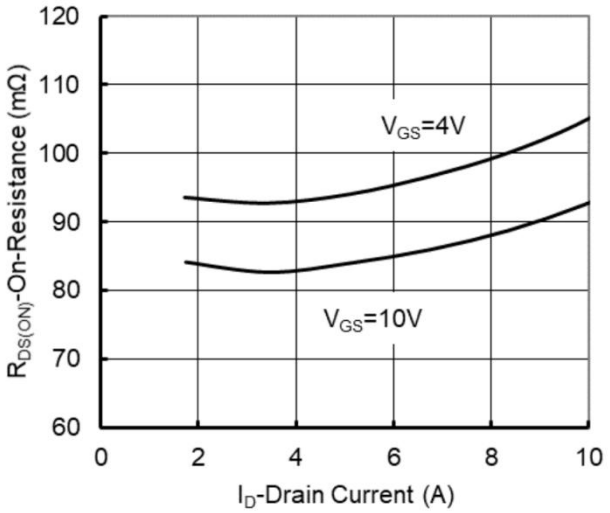


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

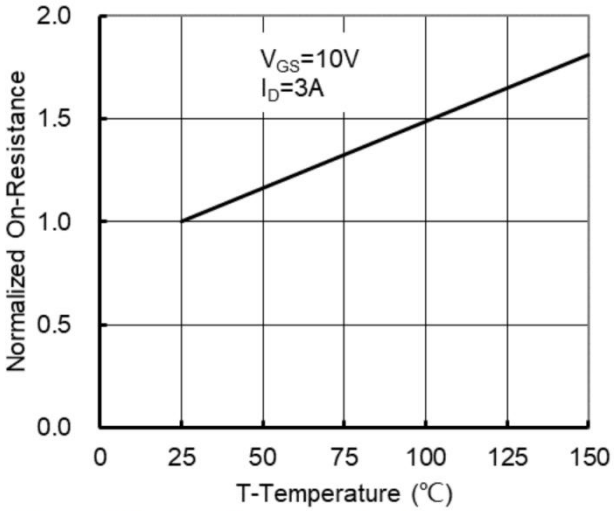


Figure 4: On-Resistance vs. Junction Temperature

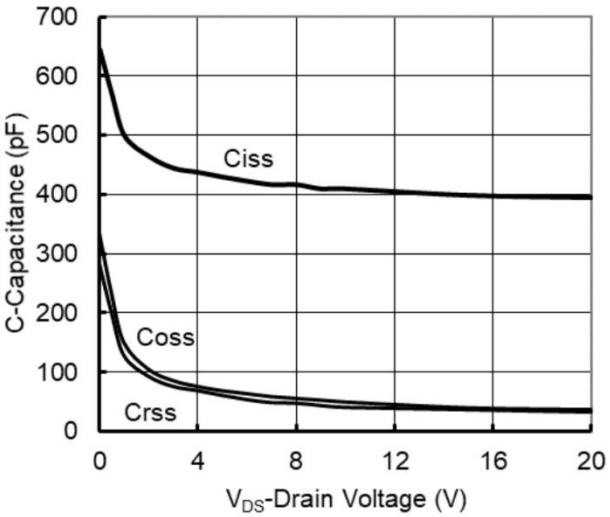


Figure5. Capacitance Characteristics

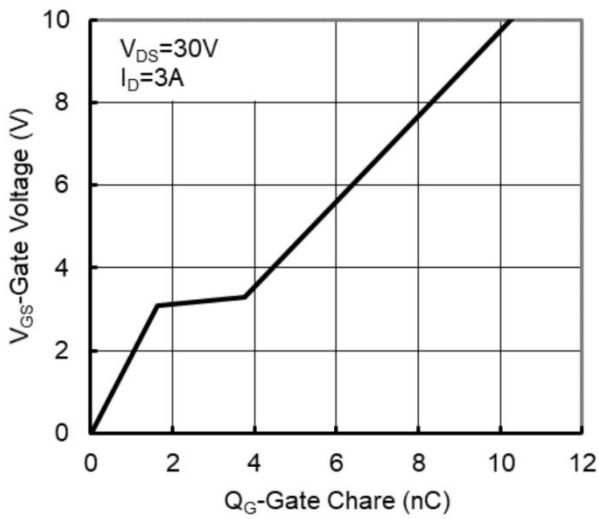


Figure6. Gate Charge

Typical Characteristics

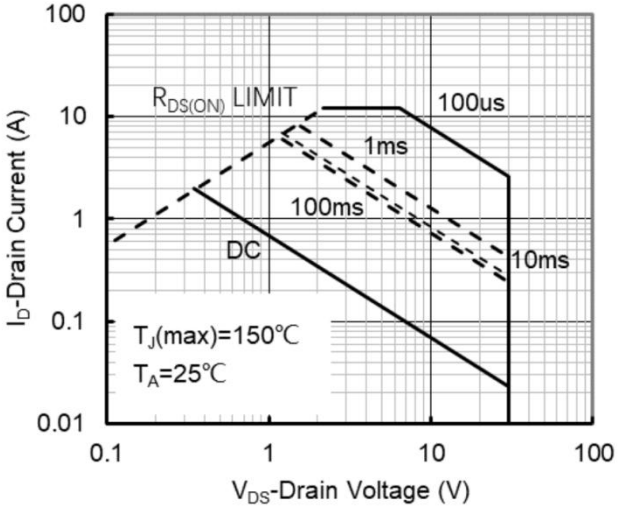


Figure7. Safe Operation Area

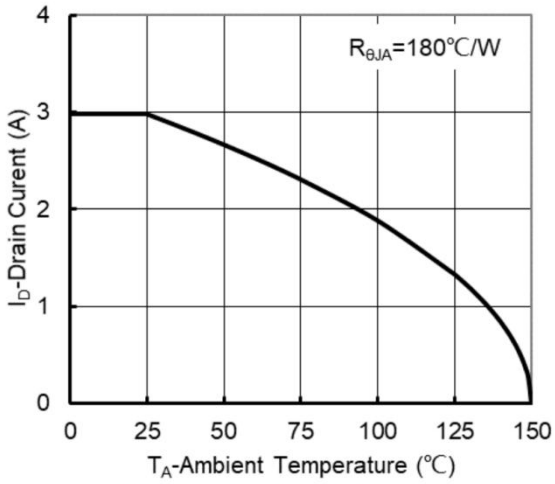


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

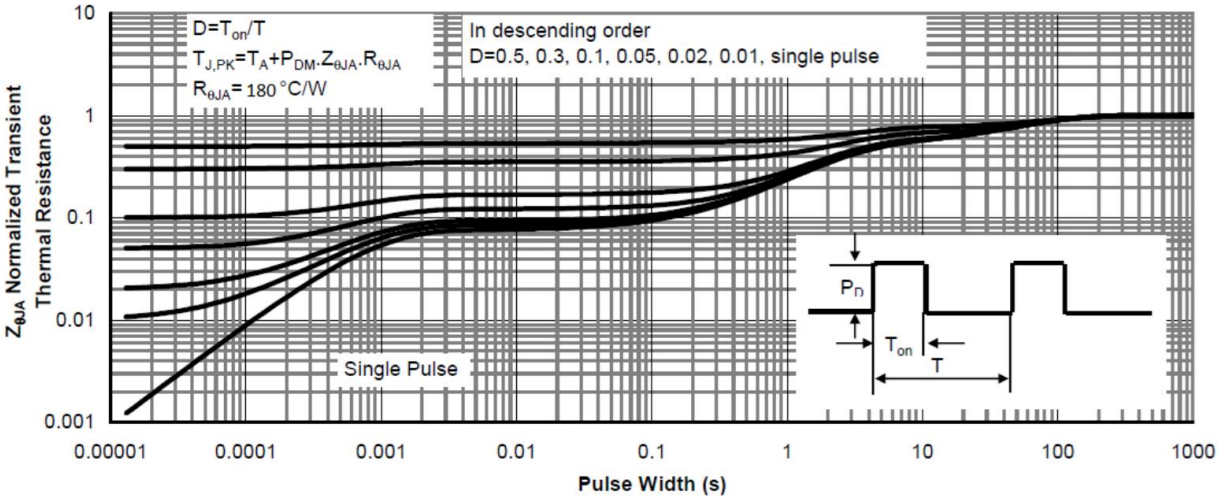
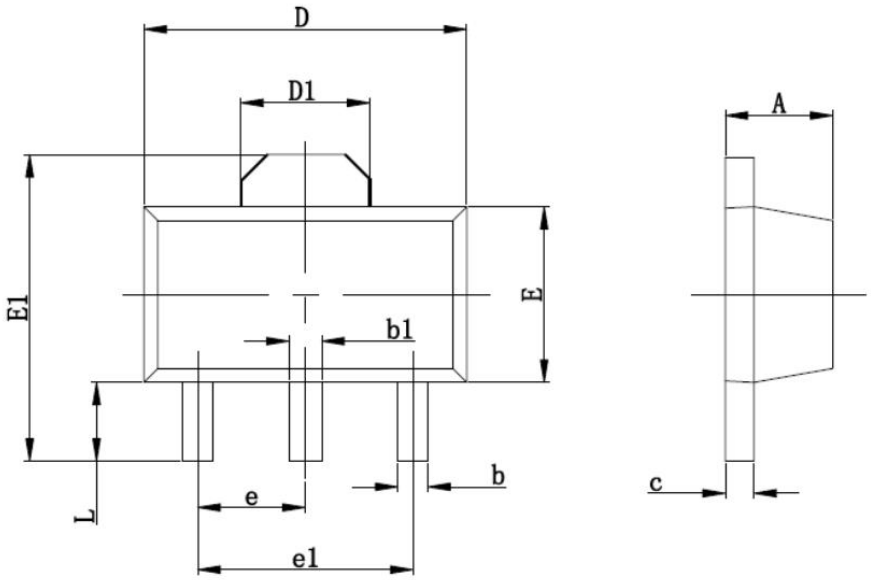


Figure9. Normalized Maximum Transient Thermal Impedance

SOT-89 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.330	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.300	4.700	0.169	0.185
D1	1.550 TYP		0.061 TYP	
E	2.250	2.650	0.089	0.104
E1	3.910	4.350	0.154	0.171
e	1.500 TYP		0.060 TYP	
e1	3.000 TYP		0.118 TYP	
L	0.800	1.200	0.031	0.047